



The Future of Analog IC Technology®

MP2949A

Tri-Loop Digital Multi-Phase Controller with PMBus Interface for IMVP8/9

DESCRIPTION

The MP2949A is a triple-rail, digital, multi-phase controller for the Core/GT/SA rails of both Intel IMVP8 and IMVP9 processor platforms. The MP2949A can work with MPS's Intelli-Phase products and traditional discrete drivers plus MOSFET structures to complete the multi-phase VR solution with minimum external components. The MP2949A is scalable up to six phases between three separated outputs.

The MP2949A provides an on-chip multiple-time programmer (MTP) to store and restore device configurations. Device configurations and fault parameters can be programmed or monitored easily using the PMBus interface. The MP2949A can monitor and report output current through the CS output from either Intelli-Phase products or the MPS driver.

The MP2949A is based on a unique, digital, multi-phase, non-linear control to provide fast transient response to a load step with a minimal number of output capacitors. With only one power loop control method for both the steady state and load transient, power loop compensation is very easy to configure without back-and-forth testing and adjusting.

The MP2949A also provides active current balancing and auto-phase shedding for better thermal and efficiency performance. The MP2949A includes input and output voltage, power (PSYS), output current (IMON), temperature monitoring with selectable protection functions, and programmable load line for each rail.

The MP2949A is available in an RoHS compliant QFN-48 (6mmx6mm) package.

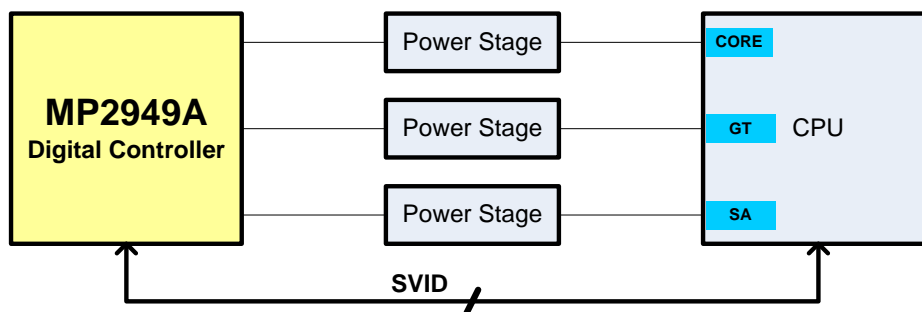
FEATURES

- Up to 6-Phase Triple-Rail Digital PWM Controller
- Configurable Phase Number: 3+2+1, 4+1+1, 2+1+1, 1+1+1, etc.
- Intel's IMVP8 and IMVP9 Compliant
- PMBus Compliant for Programming and Monitoring
- Serial VID Interface
- Built-In MTP to Store Customer Configuration
- Automatic Loop Compensation
- Fewer External Components than Conventional Analog Controller
- Auto-Phase Shedding to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing
- Input and Output Voltage and Power, Output Current Monitoring
- Regulator Temperature Monitoring
- UVLO/OVP/OTP/OCV/OTP/RVP with No Action, Latch, Retry, or Hiccup Options
- Digital Programmable Load Line
- Available in a QFN-48 (6mmx6mm) Package

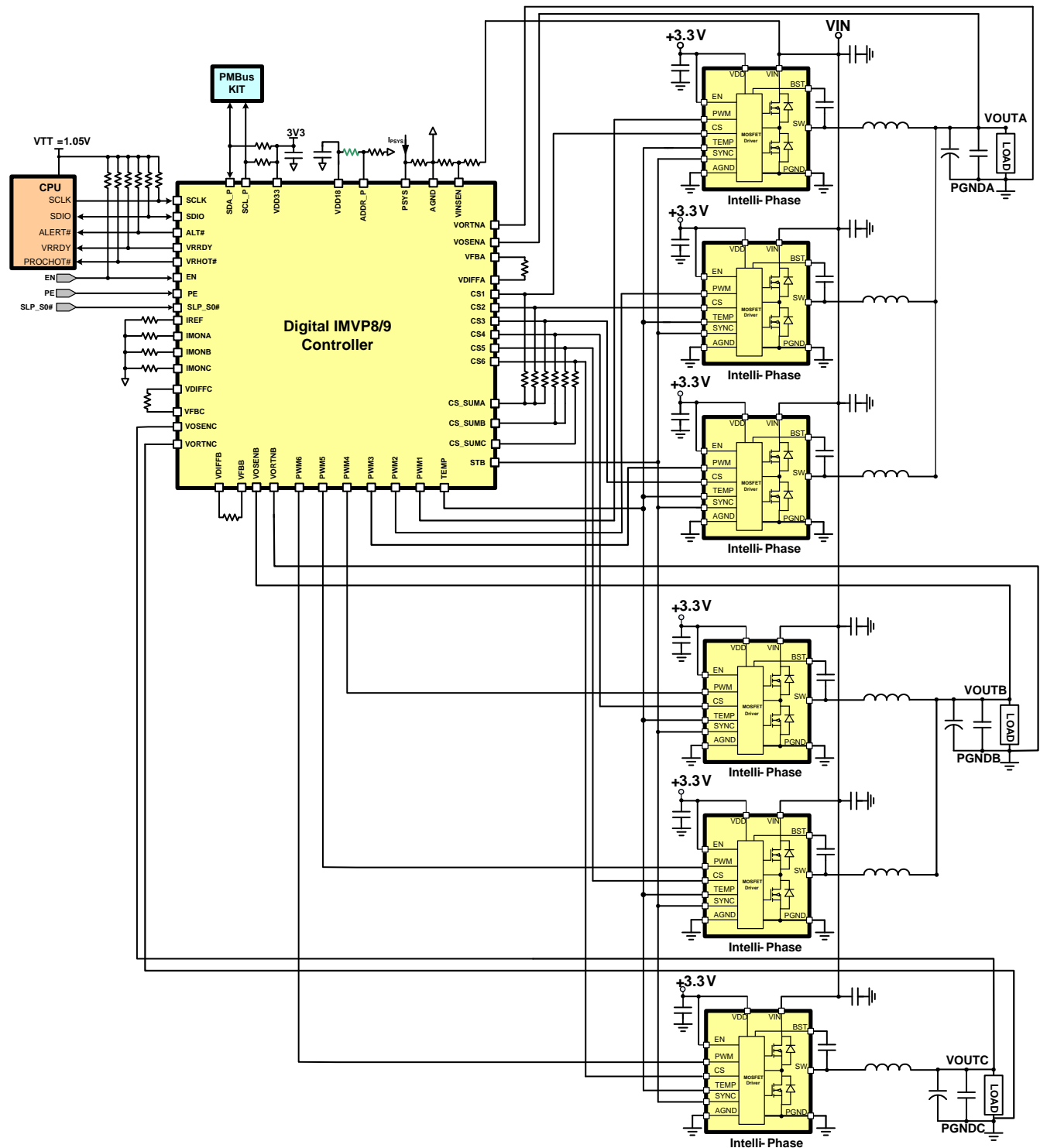
APPLICATIONS

- Notebooks/Ultrabook Cores
- Desktop Cores
- Micro Server Cores
- Tablet Cores

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

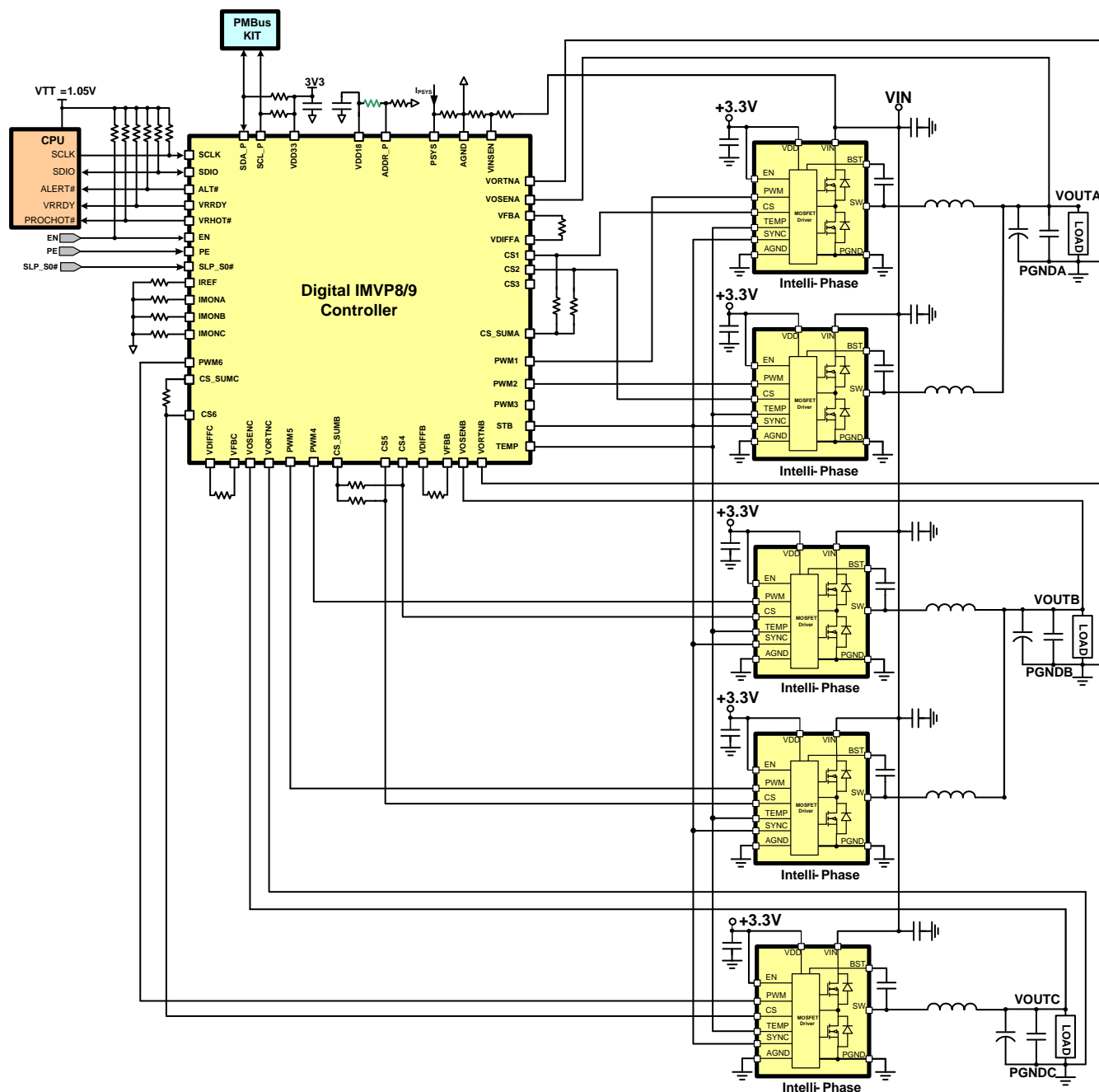


TYPICAL APPLICATION



3+2+1 Solution for VccGT, Vcore, and VccSA

TYPICAL APPLICATION (continued)



2+2+1 Solution for VccGT, Vcore, and VccSA

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2949AGQKT-xxxx**	TQFN-48 (6mmx6mm)	See Below

* For Tape & Reel, add suffix -Z (e.g. MP2949AGQKT-xxxx-Z)

** “xxxx” is the configuration code identifier for the register settings stored in the internal non-volatile memory (NVM). Each “x” can be a hexadecimal value between 0 and F. Please work with an MPS FAE to create this unique number.

TOP MARKING

MPSYYWW
MP2949A
LLLLLLLLLL

MP: MPS prefix

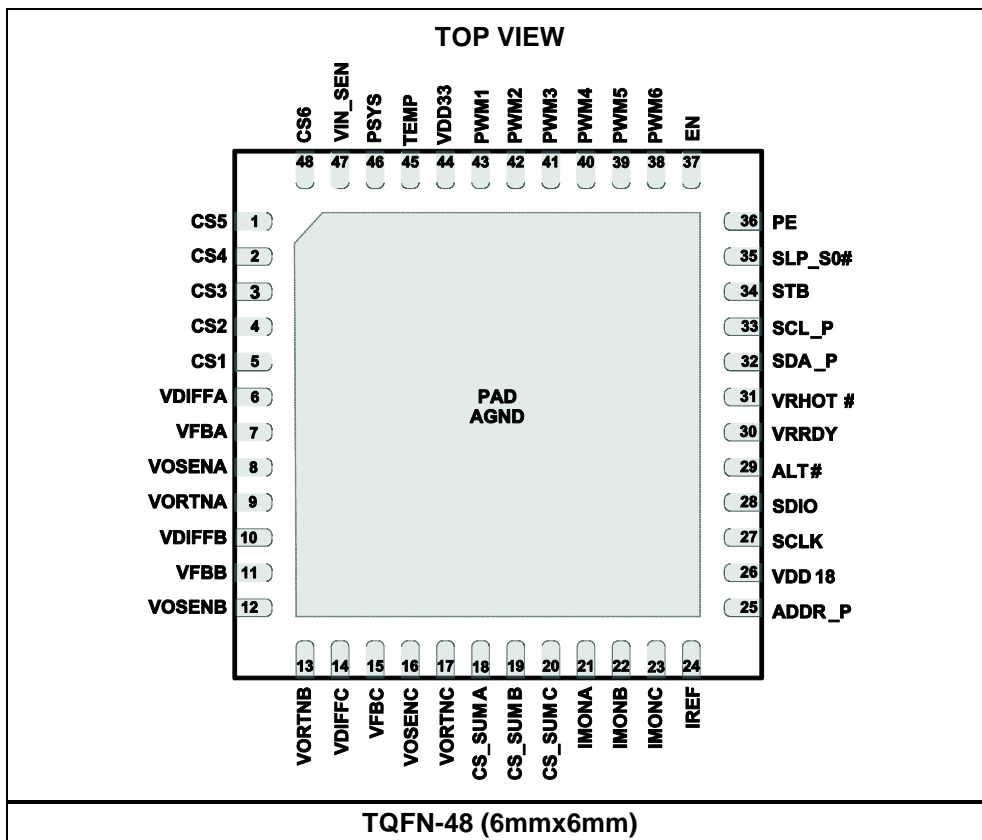
YY: Year code

WW: Week code

MP2949A: Product code of MP2949AGQKT

LLLLLLLLLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

VDD33	-0.3V to +4.5V
VDD18	-0.3V to +2.5V
VORTNA/B/C	-0.3V to +0.3V
CS1 to CS6, PWM1 to PWM6, VFBA/B/C, VDIFFA/B/C, VOSENA/B/C, VRRDY, VRHOT# SCL_P, SDA_P, PE, EN, SLP_S0#, STB	-0.3V to +3.6 V
All other pins	-0.3V to +1.8 V
Continuous power dissipation (T _A = +25°C) ⁽²⁾	3.4W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

VDD33	+3.15V to +3.4V
Operating junction temp. (T _J) ..	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
TQFN-48 (6mmx6mm)	36.....	5 °C/W

NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation produces an cause excessive die temperature.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 6-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD33 = 3.3V, EN = 1V, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Remote Sense Amplifier						
Bandwidth ⁽⁵⁾	GBW _(RSA)			20		MHz
VOSENA/B/C current	I _{VOSENA/B/C}	EN = PE = 0, V _{ORTNA/B/C} = 0V, V _{OSENA/B/C} = 3.6V		60	100	μA
Oscillator						
Frequency	f _{OSC}	R _{IREF} = 61.9kΩ		1.59		MHz
System Interface Control Inputs						
EN/PE						
Input low voltage	V _{IL(EN)}				0.4	V
Input high voltage	V _{IH(EN)}		0.9			V
Input low voltage	V _{IL(PE)}				0.8	V
Input high voltage	V _{IH(PE)}		2.4			V
Enable high leakage	I _{IH(EN)}	EN = 3.6V		3	8	μA
PE high leakage	I _{IH(PE)}	PE = 3.6V			2	μA
Enable delay	T _A	EN high to SVID ready		1.6	2.5	ms
Thermal Throttling Control						
VRHOT# low output impedance		I _{VRHOT#} = 20mA		8.5		Ω
VRHOT# high leakage current		V _{VRHOT#} = 3.6V	-3		3	μA
IMONA/B/C Output						
Current gain accuracy	I _{CS_SUM} /I _{MON}	Measured from I _{CS_SUM} to I _{MON} , T _A = 25°C	31.68	32	32.32	A/A
Comparator (Rail A/B/C Protection)						
Under-voltage threshold	V _{OSEN(UV)}	Relative to V _{OUT} setting = 2V		1.72		V
Over-voltage threshold	V _{OSEN(OV2)}	Relative to V _{OUT} setting = 2V		2.4		V
	V _{DIFF(OV1)}	OV1 DAC range			2	V
PWM1 ~ PWM6, STB Outputs						
Output low voltage	V _{OL(PWM)}	I _{PWM(SINK)} = 400μA		10	100	mV
Output high voltage	V _{OH(PWM)}	I _{PWM(SOURCE)} = -400μA	3.15			V
Rise and fall time ⁽⁵⁾		C = 10pF		10		ns
PWM/STB tri-state leakage		PWM = 1.5V, STB = 1.8V, EN = 0V	-1		1	μA
Internal LDO Output						
LDO output voltage	VDD18	I _{VDD18} = 0mA		1.8		V
LDO regulator load regulation		I _{VDD18} = 40mA		1.5	5	%

ELECTRICAL CHARACTERISTICS (continued)

VDD33 = 3.3V, EN = 1V, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VDD33 Supply						
Supply current	I _{VDD33}	EN = PE = high, VDD33 = 3.6V		13	15	mA
		EN = PE = low, VDD33 = 3.6V		70		μA
		EN = PE = high, VDD33 = 3.6V, PS4, T _A = 25°C		130	160	μA
UVLO threshold voltage	VDD33 _{UVLO}	VDD33 rising	3			V
SVID Interface						
CPU interface voltage (SDIO, SCLK)	V _{IL}	Logic low			0.45	V
	V _{IH}	Logic high	0.65			V
Leakage current (SDIO, SCLK, ALT#)	I _L	V _{TT} = 1.8V	-10		10	μA
Buffer on resistance (SDIO, ALT#) ⁽⁵⁾	R _{ON}		4		13	Ω
Maximum voltage (SDIO, SCLK, ALT#) ⁽⁵⁾	V _{MAX}	Transient voltage including ringing	-0.3		2.1	V
ADC						
ADC voltage reference		T _A = 25°C	1.592	1.6	1.608	V
ADC resolution ⁽⁵⁾				10		bits
DNL ⁽⁵⁾					1	LSB
Sample rate ⁽⁵⁾				780		kHz
DAC (Reference Voltage for Rail A/B/C)						
DAC voltage reference				1.6		V
Resolution/LSB	Δ _{DAC}			5		mV
DAC (V_{OUT} Calibration for Rail A/B/C)						
V _{osen} range				130		mV
Resolution ⁽⁵⁾				8		bit
DAC (Protection for Rail A/B/C Phase Current)						
Range	F _{SDAC_PRT}	Adjustable via PMBus	1.4		2.4	V
Resolution/LSB ⁽⁵⁾	Δ _{DAC_PRT}			10		mV
PMBus DC Characteristics (SDA_P, SCL_P)						
Input high voltage	V _{IH}	SCL_P, SDA_P	2.1			V
Input low voltage	V _{IL}	SCL_P, SDA_P			0.8	V
Input leakage current		SCL_P = SDA_P = 3.6V	-10		10	μA
Pin capacitance ⁽⁵⁾	C _{PIN}				10	pF

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 1V, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PMBus Timing Characteristics ⁽⁵⁾						
Operating frequency range			10		2000	kHz
Bus free time		Between stop and start condition	4.7			μs
Holding time			4.0			μs
Repeated start condition set-up time			4.7			μs
Stop condition set-up time			4.0			μs
Data hold time			300			ns
Data set-up time			250			ns
Clock low time out			25		35	ms
Clock low period			4.7			μs
Clock high period			4.0		50	μs
Clock/data fall time					300	μs
Clock/data rise time					1000	μs

NOTE:

5) Guaranteed by design or characterization data, not tested in production.

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	CS5	A [I]	Phase 5 current sense input. Float CS of the unused phase.
2	CS4	A [I]	Phase 4 current sense input. Float CS of the unused phase.
3	CS3	A [I]	Phase 3 current sense input. Float CS of the unused phase.
4	CS2	A [I]	Phase 2 current sense input. Float CS of the unused phase.
5	CS1	A [I]	Phase 1 current sense input. Float CS of the unused phase.
6	VDIFFA	A[O]	Differential remote sense amplifier output of Rail A.
7	VFBA	A [I/O]	Feedback of Rail A. VFBA sources a current proportional to the sensed output current. This current flows through the resistor between VFBA and VDIFFA to create a voltage drop proportional to the load current. Place a resistor between VDIFFA and VFBA to set a proper load line for Rail A.
8	VOSENA	A[I]	Positive remote voltage sense input of Rail A. VOSENA is connected directly to the VR output voltage at the load and should be routed differentially with VORTNA.
9	VORTNA	A[I]	Remote voltage sensing return input of Rail A. VORTNA is connected directly to ground at the load and should be routed differentially with VOSENA.
10	VDIFFB	A[O]	Differential remote sense amplifier output of Rail B.
11	VFBB	A [I/O]	Feedback of Rail B. VFBB sources a current proportional to the sensed output current. This current flows through the resistor between VFBB and VDIFFB to create a voltage drop proportional to the load current. Place a resistor between VDIFFB and VFBB to set a proper load line for Rail B.
12	VOSENB	A[I]	Positive remote voltage sense input of Rail B. VOSENB is connected directly to the VR output voltage at the load and should be routed differentially with VORTNB.
13	VORTNB	A[I]	Remote voltage sensing return input of Rail B. VORTNB is connected directly to ground at the load and should be routed differentially with VOSENB.
14	VDIFFC	A[O]	Differential remote sense amplifier output of Rail C.
15	VFBC	A [I/O]	Feedback of Rail C. VFBC sources a current proportional to the sensed output current. This current flows through the resistor between VFBC and VDIFFC to create a voltage drop proportional to the load current. Place a resistor between VDIFFC and VFBC to set a proper load line for Rail C.
16	VOSENC	A[I]	Positive remote voltage sense input of Rail C. VOSENC is connected directly to the VR output voltage at the load and should be routed differentially with VORTNC.
17	VORTNC	A[I]	Remote voltage sensing return input of Rail C. VORTNC is connected directly to ground at the load and should be routed differentially with VOSENC.
18	CS_SUMA	A [I]	Total phase current monitor for Rail A AVP. Connect the active phase CS signal together to CS_SUMA through current sense resistors.
19	CS_SUMB	A [I]	Total phase current monitor for Rail B AVP. Connect the active phase CS signal together to CS_SUMB through current sense resistors.
20	CS_SUMC	A [I]	Total phase current monitor for Rail C AVP. Connect the active phase CS signal together to CS_SUMC through current sense resistors.

PIN FUNCTIONS *(continued)*

Pin #	Name	I/O	Description
21	IMONA	A [I/O]	Analog total load current signal of Rail A. IMONA sources a current proportional to the sensed total load current from CS_SUMA. Connect an external resistor from IMONA to AGND to program the output current report gain.
22	IMONB	A [I/O]	Analog total load current signal of Rail B. IMONB sources a current proportional to the sensed total load current from CS_SUMB. Connect an external resistor from IMONB to AGND to program the output current report gain.
23	IMONC	A [I/O]	Analog total load current signal of Rail C. IMONC sources a current proportional to the sensed total load current from CS_SUMC. Connect an external resistor from IMONC to AGND to program the output current report gain.
24	IREF	A [I/O]	Internal bias current set. Connect a 61.9kΩ resistor from IREF to AGND.
25	ADDR_P	A [I/O]	PMBus address setting.
26	VDD18	A [I/O]	1.8V LDO output for internal digital power supply. Connect a 1μF bypass capacitor to AGND.
27	SCLK	D [I]	Source synchronous clock from the CPU. The SCLK frequency range is 10 - 26.25MHz.
28	SDIO	D [I/O]	Data signal between CPU and VID controller.
29	ALT#	D [O]	Alert. ALT# is an open-drain output. The ALT# signal is from the VR controller to the CPU.
30	VRRDY	D [O]	VR ready output of the controller. VRRDY is an open-drain output that signals when the output voltage is outside of the proper operating range. VRRDY pulls up to 1.0V, but some systems may pull VRRDY up to a maximum voltage of 3.3V with external pull-up resistors.
31	VRHOT#	D [O]	Voltage regulator thermal throttling logic output. VRHOT# is an open-drain output. VRHOT# pulls low actively if the monitored temperature exceeds the programmed VRHOT# temperature threshold or PSYS exceeds the critical level in IMVP9. Pull VRHOT# up to 1V through a 10kΩ resistor.
32	SDA_P	D [I/O]	Data signal between PMBus controller and VID controller.
33	SCL_P	D [I]	Source synchronous clock from PMBus controller.
34	STB	D [O]	Digital output to tell Intelli-Phase to enter low-power mode.
35	SLP_S0#	D [I]	Control SVID communication between the VID controller and CPU in PS4 mode. Pull SLP_S0# to 3V3 with a 100kΩ resistor if it is not being used.
36	PE	D [I]	Program enable. PE is the program enable input for system configuration through the PMBus when EN is off. Pull PE low to AGND with a 0Ω resistor if it is not being used.
37	EN	D [I]	Enable control for the controller.
38	PWM6	D [O]	Tri-state logic level PWM outputs. Each output is connected to the input of the Intelli-Phase's PWM pin. The logic levels are 0V for low logic and 3.3V for high logic. The output is set to tri-state to shut down both the high-side MOSFET and low-side MOSFET of the Intelli-Phase.
39	PWM5	D [O]	
40	PWM4	D [O]	
41	PWM3	D [O]	
42	PWM2	D [O]	
43	PWM1	D [O]	
44	VDD33	A [I]	3.3V power supply input. Connect a 4.7μF bypass capacitor from VDD33 to AGND.

PIN FUNCTIONS *(continued)*

Pin #	Name	I/O	Description
45	TEMP	A [I]	Analog signal from the VR to the VID controller. TEMP indicates the power stage temperature. Connect all of MPS Intelli-Phase's VTEMP pins together to produce the maximum junction temperature. Then connect these VTEMP pins to MP2949A's TEMP pin. A 49.9k Ω resistor in parallel with a 1 μ F capacitor from TEMP to AGND is needed to discharge the TEMP voltage.
46	PSYS	A[I]	System total input power sensing. A current proportional to the system power flows out from a sensor to ground through a PSYS resistor (R _{PSYS}) to AGND.
47	VIN_SEN	A[I]	Input voltage sense. Connect VIN_SEN to V _{IN} through a 1/16 divider network.
48	CS6	A [I]	Phase 6 current sense input. Float CS of the unused phase.
Pad	AGND	I/O	Analog ground.

BLOCK DIAGRAM

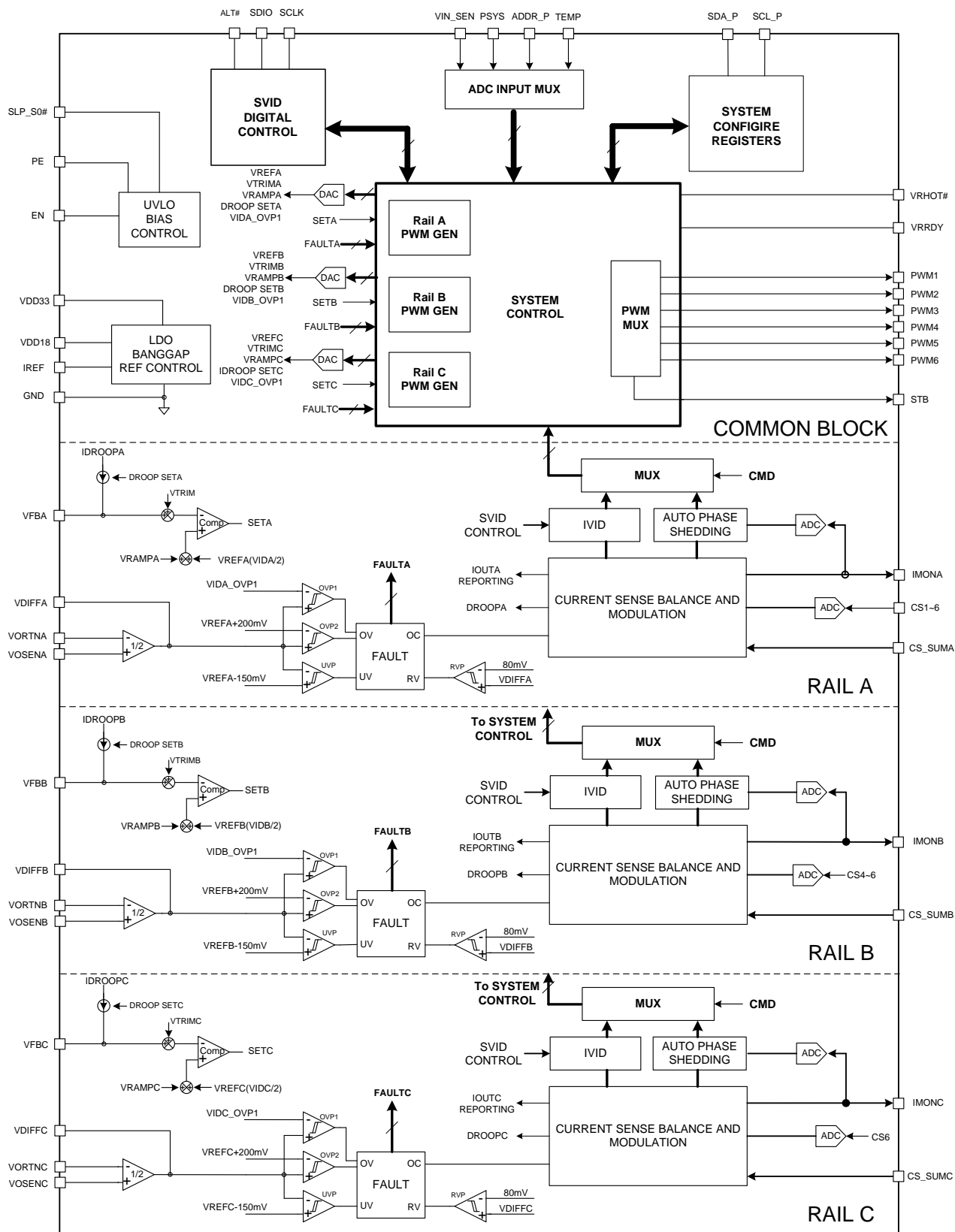


Figure 1: Functional Block Diagram

OPERATION

The MP2949A is a digital, multi-phase, Intel IMVP8/9 compliant voltage regulator (VR) controller with up to three output rails. The MP2949A is scalable up to six phases between three separated outputs with variable combinations through the register setting, making the MP2949A able to support Intel's Y/U/H/S lines of VR design. Auto-phase shedding is done according to the load current to improve VR efficiency. The MP2949A contains blocks of PMBus and SVID interface, precision DAC and ADC, MTP for custom configuration, differential remote voltage sense amplifier, fast comparators, current sense amplifiers, internal slope compensation, VR_READY monitor and temperature monitor. The MP2949A also makes the digital multi-phase controller provide the smallest BOM cost for the VR solution with a very easy and flexible design progress. Fault protection features include V_{IN} under-voltage lockout (UVLO), over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), over-temperature protection (OTP), and reverse-voltage protection (RVP).

System Rail and Phase Configuration

The MP2949A can support multiple rails and phases depending on different applications or platforms. The MP2949A can be configured up to six phases for Rail A, up to two phases for Rail B, and one phase for Rail C operation applications via the PMBus register MFR_PHASE_CFG (CAh[4:0]) (see Table 1).

The MP2949A provides the design flexibility to enable or disable the reserved phase without a soldering process. If the design has been previously set with the 1+2+1 solution, then by setting CAh, the MP2949A can support the 1+1+1 solution directly without any configuration on the Intelli-Phase side.

The control bit (CAh[7:5]) can disable the unused rail, and the control bit (CBh[15]) can disable the PWMx (x > 1) of Rail A. The unused PWM enters tri-state. The active phase interleaves automatically. Only the PWM on the enabled rail and MFR_PHASE_CFG enabled are active.

Table 1: Phase Configuration and Active PWM Pins (CBh[15], Default 1)

MFR_PHASE_CFG[4:0]	Active PWM Pins		
	Rail A	Rail B	Rail C
00000	1, 2, 3, 4, 5, 6	-	-
00001	1, 2, 3, 4, 6	5	-
00010	1, 2, 3, 4, 6	-	-
00011	1, 2, 3, 4	5, 6	-
00100	1, 2, 3, 4	5	6
00101	1, 2, 3, 4	5	-
00110	1, 2, 3, 4	-	-
00111	1, 2, 3	4, 5	6
01000	1, 2, 3	4, 5	-
01001	1, 2, 3	5	6
01010	1, 2, 3	5	-
01011	1, 2, 3	-	-
01100	1, 2	4, 5	6
01101	1, 2	4, 5	-
01110	1, 2	5	6
01111	1, 2	5	-
10000	1, 2	-	-
10001	1	5	6
10010	1	5	-
10011	1	-	-
Others	Not supported		

PMBus Address

To support multiple VR devices used with the same PMBus interface, there is a PMBus address for every device. The PMBus address is a 7-bit code. The MSB 3-bit is set up by the register, and the lower 4-bit address can either be set up by the register or the resistor. The register SHUTLEVEL_ADDRPMBUS (E1h[6:0]) and ADDR_P can be used to program the PMBus address (see Figure 2). Use two resistor dividers connected from VDD18 and ground to get the setting voltage for the corresponding address. Table 2 explains how the PMBus address is set by the external voltage with the default E1h[6:4] = 010 b.

The default setting on the external resistor is $R_a = \text{NS}$ and $R_b = 0\Omega$, where the default PMBus address is 20h.

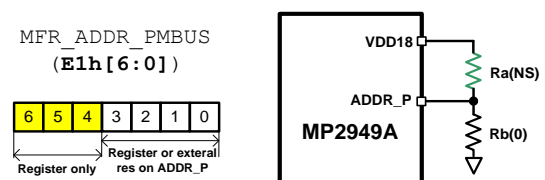


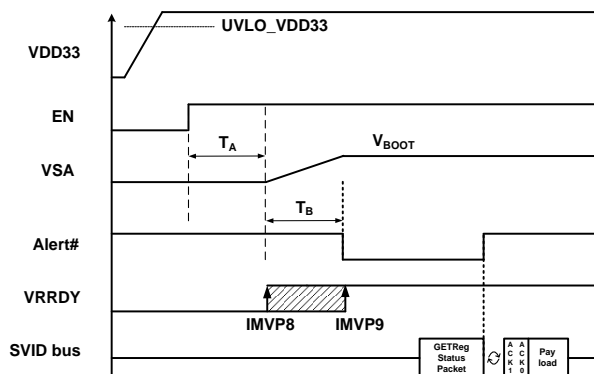
Figure 2: PMBus Address Setting

Table 2: PMBus Address Setting by ADDR_P Voltage

PMBus Address	Recommended Setting Voltage (V)	Min Setting Voltage (V)	Max Setting Voltage (V)
20h	0	0	0
21h	0.03	0.027	0.033
22h	0.0588	0.053	0.065
23h	0.0844	0.076	0.093
24h	0.1152	0.104	0.127
25h	0.1574	0.142	0.174
26h	0.204	0.184	0.225
27h	0.266	0.24	0.293
28h	0.338	0.305	0.373
29h	0.43	0.388	0.474
2Ah	0.54	0.487	0.595
2Bh	0.672	0.606	0.741
2Ch	0.844	0.762	0.931
2Dh	1.046	0.944	1.153
2Eh	1.298	1.171	1.431
2Fh	1.6	1.455	1.6

Power-On Sequence

The MP2949A is supplied by a +3.3V voltage for analog circuits. The system is reset by the internal power-on reset signal (POR). After the system exits POR, the data in the MTP is loaded to the registers to configure the VR operation. The initialization process takes about 0.7ms (T_A in Figure 3). Then the soft-start process is executed to charge the output capacitor with the SetVID_Slow slew rate until the reference reaches the target boot voltage (T_B in Figure 3) set by $V_{BOOT}/Slow$.


Figure 3: Start-Up Sequence

The MP2949A supports both IMVP8 and IMVP9 with different VRRDY asserting time settings. The VRRDY signal asserts either when the SVID interface is ready to receive CPU commands (IMVP8) or when the VR reaches the boot voltage level (IMVP9).

The MP2949A also provides additional programmable EN delay by setting registers MFR_EN_DLY (FBh[6:0]) and MFR_EN_FILTER_TIME (FBh[10:7]). T_A can be set longer than the 0.7ms (i.e.: $T_A = 0.7ms + MFR_EN_DLY + MFR_EN_FLT_TIME$). See the Register Map section on page 75 for details on programming the delay.

For rails where the boot voltage is set to 0, the PWM of the rail remains in tri-state until a valid SVID voltage is received. The controller then ramps the voltage to the target value and asserts ALT#.

Steady State and Switching Frequency

The MP2949A applies a digital, non-linear control to provide a fast transient response and easy loop compensation. The duty cycle of each active phase's PWM updates in real time according to the input voltage and reference voltage under the set switching frequency. The active phases are interleaved automatically during steady state. In steady state, the switching frequency is set at MFR_FS_VBOOT (E5h[14:8]).

The MP2949A changes the switching frequency of individual phases adaptively during load transient to achieve super-fast transient performance with minimal BOM cost.

Power State Change

The SVID bus can switch the VR to different power states (PS0, PS1, PS2, PS3, and PS4) to achieve optimized efficiency on various load conditions. These states are entered by programming the power state register using SVID's set power state command. The VR then optimizes its power loss to flatten the efficiency curve over the operating current range with the power state commands issued by the processor. In PS0 mode, all phases run in continuous conduction mode (CCM). In PS1 mode, only one phase runs in CCM, and the other phases are in tri-state. In PS2 mode, only one phase is running in diode emulation mode, and the

switching frequency drops automatically to save power loss at light load. See Table 3 for details on how the phases act in different power states.

Table 3: Power State and Phase Activities

PS State	Active Phase	CCM/DCM
PS0	All phases PWM	CCM
PS1	One phase PWM	CCM
PS2	One phase PWM	DCM
PS3	One phase PWM	DCM
PS4	All off	-

During the dynamic VID transition issued by the SVID commands, such as SetVID_Fast or SetVID_Slow, the power state is changed to PS0 by default and runs in full-phase PWM mode. After the output is well-regulated to the new target voltage, the power state remains in PS0 mode until the processor sends a new command to change the power state.

Reference

The MP2949A supports both 5mV VID step and 10mV VID step for IMVP8 and IMVP9 with only one DAC for each rail to generate REF. A control bit (MFR_STEP_SEL_R1) in register E4h chooses the VID step. If this control bit is written to 1, then calculate the output (V_{REF}) of the DAC with Equation (1):

$$V_{REF} = (VID + 49) / 2 * 5mV \quad (1)$$

Calculate V_{REF} when the control bit is written to 0 with Equation (2):

$$V_{REF} = (VID + 19) / 2 * 10mV \quad (2)$$

Output Voltage Sense

The output voltages of the three rails are sensed remotely with a 1/2 gain differential amplifier. The sensed output voltages are used for closed-loop compensation, over-, under-, and reverse-voltage (OV, UV, RV) protection, and PMBus monitoring. A proper package sense is recommended to enclose the board parasitic within the feedback loop of the VR for noise rejection and performance optimization (see Figure 4). Two 0Ω resistors are placed close to the MP2949A. To avoid errant operation or board damage when the CPU is absent, two 100Ω catch-up resistors are connected to the V_{OUT} and PGND plane to get the output feedback, even if the CPU is absent.

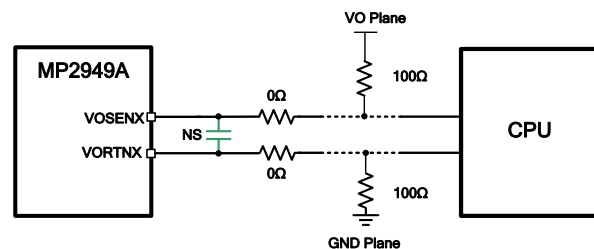


Figure 4: Output Remote Sense

Input Voltage Sense

The input power supply voltage is sampled at VIN_SEN and used for output voltage regulation as the feed-forward control, V_{IN} UVLO and V_{IN} OVP fault protection, and monitoring via the PMBus. Use two resistors connected to the input voltage and a 10nF bypass capacitor to get a 1/16 divider for VIN_SEN (see Figure 5). The default values are $R_{VIN_1} = 2M\Omega$ and $R_{VIN_2} = 133k\Omega$.

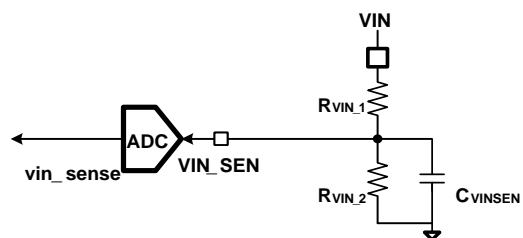


Figure 5: V_{IN} Sense Network

Current Sense

The MP2949A works with the MPS Intelli-Phase to sense per-phase inductor current and total current easily (see Figure 6). The cycle-by-cycle current information is used for phase current balancing, over-current protection, and load-line setting. The current sense gain is called K_{CS} in Intelli-Phase products. The resistor (R_{CS}) is connected from CS to CS_SUM. CS_SUM is a 1.23V constant voltage, which is capable of sinking small currents to provide voltage shifts that meet the CS operating voltage range.

Different Intelli-Phase products have different operating voltage ranges of CS, V_{CS_MIN} , and V_{CS_MAX} . Refer to each Intelli-Phase's datasheet to determine the minimum and maximum operating voltage range. Determine a proper R_{CS} value with Equation (3):

$$V_{CS_MIN} < I_{CS} R_{CS} + 1.23V < V_{CS_MAX} \quad (3)$$

$$I_{CS} = IL \times K_{CS}$$

By working with the Intelli-Phase, the MP2949A does not need temperature compensation and impedance matching to achieve an accurate current sense.

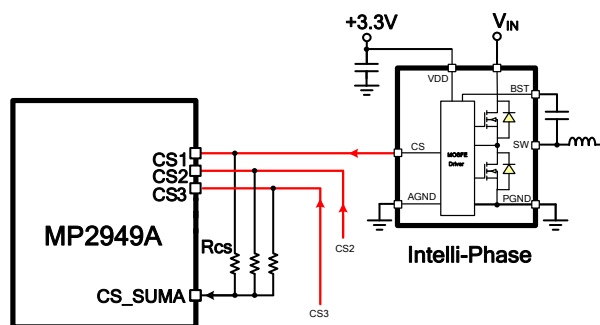


Figure 6: Phase Current Sense with 3-Phase Configuration

IMON and IDROOP

The current flowing out from IMON, called ISUM, is 1/32 of the filtered CS_SUM. Place a resistor from IMON to ground to generate a voltage proportional to the output current. The IMON voltage is sampled and converted by ADC and then stored in the I_{OUT} register, which is scaled to the ICCMAX = ADC full range (FFh). The IMON voltage reaches its max data (V_{IMON_Max}) when the output current reaches ICCMAX.

The IMON voltage can be calculated with Equation (4):

$$V_{\text{IMON}} = \frac{I_{\text{OUT}} \times K_{\text{CS}} \times R_{\text{IMON}}}{32} \quad (4)$$

Where K_{CS} is the current sense gain of the Intelli-Phase, I_{OUT} is the output current, R_{IMON} is the IMON resistor, and V_{IMON_Max} is $1.6 \cdot 8 / 11V$.

R_{IMON} can be set with $I_{OUT} = ICCMAX$ and $V_{IMON} = V_{IMON_MAX}$ in Equation (5):

$$R_{\text{IMON}} = \frac{32 \times V_{\text{IMON_Max}}}{I_{\text{CCMAX}} \times K_{\text{CS}}} \quad (5)$$

Figure 7 shows the MP2949A IMON sense and IDROOP block diagram.

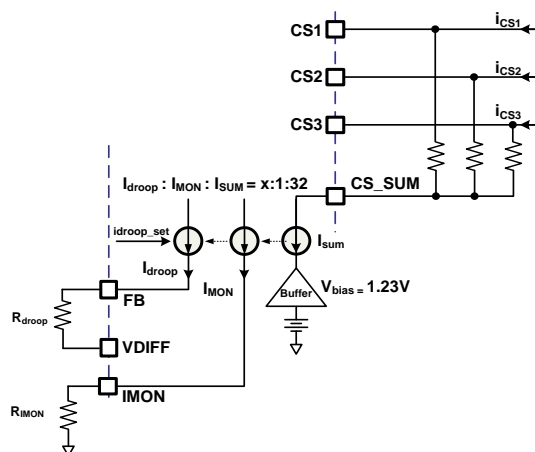


Figure 7: Current Sense IMON/IDROOP

Static Load Line Setting

The MP2949A uses a resistor between VFB and VDIFF to set the static load line. The droop current (default $1/8 * 1/2$ of ISUM) flowing through the droop resistor from VFB to VDIFF generates the droop voltage. Given the load line regulation (R_{LL}), calculate R_{DROOP} according to Equation (6):

$$R_{\text{DROOP}} = \frac{R_{\text{LL}}}{2 \times K_{\text{CS}} \times K_{\text{Droop}}} \quad (6)$$

Where the K_{CS} is the current sense gain of the Intelli-Phase (default value is $10\mu A/A$ for MP86901x series), and K_{Droop} is the gain of the droop current mirror (default is $4/8 * 1/8$).

Digital Programmable Load Line

Beside the load line setting from an external droop resistor, the MP2949A also provides a digital programmable load line trim by the register IDROOP_SET (1Bh[3:0]). The droop current mirror gain of the MP2949A is shown in Table 4. The load line can be changed through the PMBus and stored in the MTP. With a digital load line, the droop can be changed without replacing the external droop resistor. The default value of IDROOP_SET is 0001b, which presents a 1/16 gain to ISUM.

Table 4: Digital Load Line Trim

IDROOP_SET [3:0]	IDROOP Gain
0000 b	0
0001 b (default)	$4/8 * 1/8 * \text{ISUM}$
0010 b	$5/8 * 1/8 * \text{ISUM}$
0011 b	$6/8 * 1/8 * \text{ISUM}$
0100 b	$7/8 * 1/8 * \text{ISUM}$
0101 b	$8/8 * 1/8 * \text{ISUM}$
0110 b	$9/8 * 1/8 * \text{ISUM}$
0111 b	$10/8 * 1/8 * \text{ISUM}$
1000 b	$11/8 * 1/8 * \text{ISUM}$
1001 b	$12/8 * 1/8 * \text{ISUM}$
1010 b	$13/8 * 1/8 * \text{ISUM}$
1011b	$14/8 * 1/8 * \text{ISUM}$
1100 b	$15/8 * 1/8 * \text{ISUM}$
1101 b	$16/8 * 1/8 * \text{ISUM}$
1110 b	$17/8 * 1/8 * \text{ISUM}$
1111 b	$18/8 * 1/8 * \text{ISUM}$

IoT Report

The I_{OUT} register (15h) in the SVID register reports to the processor to prevent exceeding the thermal design point and maximum current capability of the system. The MP2949A applies a user-programmable register, which contains the gain, MFR_IMON_SVID_GAIN (FCh[7:0]), and a signed current offset, MFR_IMON_SVID_OFFSET (FCh[14:8]), on the SVID I_{OUT} reporting. The two programmable parameters allow the IMON scaling to match the design's voltage regulator tolerance band (VRTOB) calculation. This provides the most accurate current reporting across the entire load range and maximizes the performance of the Intel turbo. The gain can be reduced or offset to under-report the total current to the CPU for a better performance (see Figure 8). See the Register Map section on page 75 for details on how to configure register FCh.

The PMBus I_{OUT} register (8Ch) is also used for total current protection. If the auto-phase shedding function is enabled via the PMBus, the total current report is used to determine whether to enter or exit phase shedding mode to flatten the overall efficiency over the operating current range. Registers IOUT_CAL_GAIN (38h[10:0]) and IOUT_CAL_OFFSET (39h[5:0]) are used to program the PMBus I_{OUT} report gain and offset to ensure that the MP2949A tracks the load current.

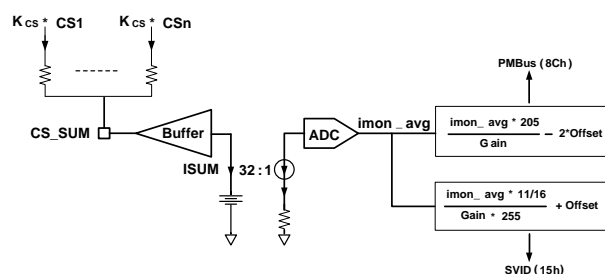


Figure 8: Total Current Sense and Report

Temperature Sense

The MP2949A measures the external temperature by connecting all Intelli-Phase VTEMP pins together (see Figure 9). The voltage of TEMP of the MP2949A is the highest voltage among the Intelli-Phase devices, which indicates the highest temperature of the VR power system. The sensed temperature is used for over-temperature fault protection or asserting the SVID thermal alert or VRHOT# signal for the processor. A 49.9kΩ resistor in parallel with a 1μF capacitor from TEMP to GND is needed to discharge TEMP.

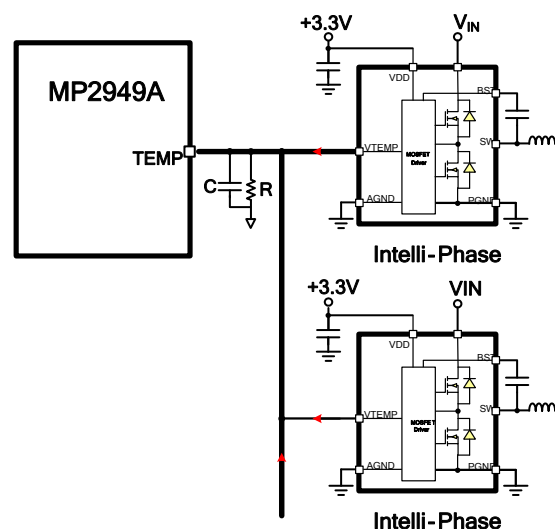


Figure 9: External Temperature Sense

VTEMP of the Intelli-Phase is a voltage output proportional to the junction temperature. The junction temperature can be calculated with Equation (7):

$$T_{\text{JUNCTION}} = \frac{V_{\text{TEMP}} + 100\text{mV}}{10\text{mV}/^{\circ}\text{C}} \quad (7)$$

for $T_{\text{JUNCTION}} > 10^{\circ}\text{C}$

For example, if VTEMP is 700mV, then the junction temperature of that Intelli-Phase is 80°C. VTEMP cannot drop below 0V, or it will read 0V for junction temperatures lower than 10°C.

Dynamic Voltage Identification (DVID)

The MP2949A supports dynamic VID change when it receives three SVID commands: SetVID_Fast, SetVID_Slow, and SetVID_Decay.

The VID slew rate of SetVID_Fast is set by register VID_STEP_NUM (FAh[7:6]), which is equal to the VID increase or decrease per step, and VID_SR_CNT (FAh[5:0]), which defines the time duration VID change one time. The fast slew rate can be calculated with Equation (8):

$$\text{SlewRate} = \frac{(\text{VID_STEP_NUM} + 1) \times \text{VID_STEP}}{\text{VID_SR_CNT} \times 100\text{ns}} \quad (8)$$

Where VID_STEP_NUM is programmable from 0 ~ 3, VID_STEP is programmable to either 5mV or 10mV according to the CPU requirement, and VID_SR_CNT is programmable from 1 to 63. If VID_STEP_NUM is 0, VID_STEP is 5mV, and VID_SR_CNT is 15, then the slew rate is 33.3mV/μs.

The SetVID_Slow slew rate is decided by register F9h[3:0], which can program to 1/2, 1/4, 1/8, or 1/16 of SetVID_Fast. The slew rate for SetVID_Decay is determined by the load current and output capacitor bank.

Another register, MFR_ALT_SET (FDh), sets the ALT# asserting time. Delay can also be added, which helps the MP2949A meet the Intel spec. See the Register Map section on page 76 for details on how to configure register FDh.

When DVID is up, the inductor current becomes higher to charge the output capacitors. This current introduces a large positive droop voltage due to the load line, resulting in an output voltage lower than the target, which may cause the output voltage to exceed the minimum regulation tolerance budget 1μs after ALT# asserts.

The MP2949A can be programmed to ramp up more VID steps by register FAh[10:8] after VID ramps to the target. Then the MP2949A keeps this VID for the time set by MFR_PLATFORM_TIME (F1h[11:6]). VID drops back to the target VID to fasten the output voltage to rise into the regulation tolerance

budget (TOB) as required by the Intel spec. See the Register Map section on page 71 for configuration details.

When the output voltage is ramping downward, the inductor current becomes smaller to discharge the output capacitors, which continue discharging the output capacitors when ramping ends and may lead to an output voltage undershoot.

The MP2949A applies a low-pass filter for the VID_DAC to smooth the reference voltage when the output voltage is ramping downward.

Auto-Phase Shedding

The MP2949A provides an auto-phase shedding function to improve efficiency at PS0 according to the comparison between the total current report and the programmable threshold.

There are three types of registers for configuring the auto-phase shedding function.

The first register, MFR_1PHL (BBh[4:0]), sets the phase shedding level for the three rails. This register is a 1-phase CCM level. 2- ~ 6-phase CCM levels is MFR_1PHL*phase_num. 1-phase DCM level is fixed at 5A.

The second register, MFR_PHASE_HYS (BCh[3:0]), sets the hysteresis current value during phase adding.

The third register, DROP_PHASE (CBh[10:8]), sets the delay time of the phase shedding action after the system total current detected is smaller than the phase shedding threshold. Once the total current is higher than the phase adding threshold, the idle phases are added in immediately (see Figure 10). See the Register Map section on page 49, page 50, and page 55 for auto-phase shedding and adding configuration details.

Table 5 and Table 6 list the phase shedding and adding entry condition based on the current report.

Table 5: Phase Number during Phase Adding Based on the Current Report (I_{OUT})

Condition	Phase Number
$5 * MFR_1PHL + MFR_PHASE_HYS \leq I_{OUT}$	6-phase CCM or full (<6) phase CCM
$4 * MFR_1PHL + MFR_PHASE_HYS \leq I_{OUT} < 5 * MFR_1PHL + MFR_PHASE_HYS$	5-phase CCM or full (<5) phase CCM
$3 * MFR_1PHL + MFR_PHASE_HYS \leq I_{OUT} < 4 * MFR_1PHL + MFR_PHASE_HYS$	4-phase CCM or full (<4) phase CCM
$2 * MFR_1PHL + MFR_PHASE_HYS \leq I_{OUT} < 3 * MFR_1PHL + MFR_PHASE_HYS$	3-phase CCM or full (<3) phase CCM
$1 * MFR_1PHL + MFR_PHASE_HYS \leq I_{OUT} < 2 * MFR_1PHL + MFR_PHASE_HYS$	2-phase CCM or full (<2) phase CCM
$5A + MFR_PHASE_HYS \leq I_{OUT} < 1 * MFR_1PHL + MFR_PHASE_HYS$	1-phase CCM
$I_{OUT} < 5A + MFR_PHASE_HYS$	1-phase DCM

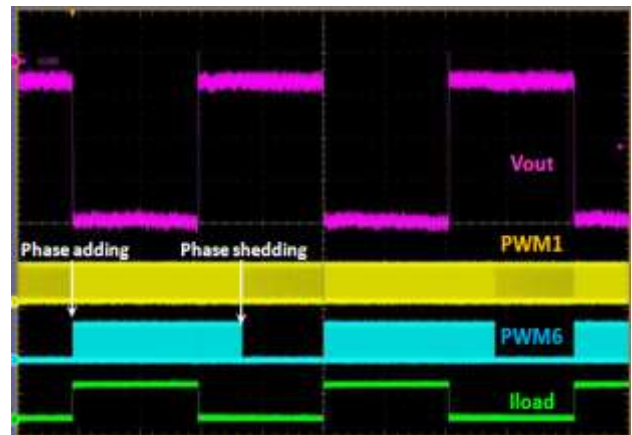
Table 6: Phase Number during Phase Shedding Based on the Current Report (I_{OUT})

Condition	Phase Number
$5 * MFR_1PHL < I_{OUT}$	6-phase CCM or full (<6) phase CCM
$4 * MFR_1PHL < I_{OUT} \leq 5 * MFR_1PHL$	5-phase CCM or full (<5) phase CCM
$3 * MFR_1PHL < I_{OUT} \leq 4 * MFR_1PHL$	4-phase CCM or full (<4) phase CCM
$2 * MFR_1PHL < I_{OUT} \leq 3 * MFR_1PHL$	3-phase CCM or full (<3) phase CCM
$1 * MFR_1PHL < I_{OUT} \leq 2 * MFR_1PHL$	2-phase CCM or full (<2) phase CCM
$5A < I_{OUT} \leq 1 * MFR_1PHL$	1-phase CCM
$I_{OUT} \leq 5A$	1-phase DCM

Besides the basic rules listed in Table 3, the following conditions must occur to improve the transient condition.

- When the configured full-phase number is smaller than the phase adding number, the system runs with the full phase.
- The DVID process runs with the full-phase number if the VR receives the SetVID_Fast or SetVID_Slow command from the processor, regardless of whether the auto-phase shedding function is enabled or disabled.
- The phase shedding process starts after the VR is settled.

Load step-up causing VFB to fall below REF - 15mV triggers the VR to run with a full phase to avoid output-voltage undershoot.


Figure 10: Phase Shedding and Adding Process

IVID

The MP2949A supports the IVID function that is defined in the IMVP8 spec for auto-phase shedding and optimizing operation for efficiency, regardless of the PS state required.

There are two types of registers for the IVID function:

1. **IVIDx-VID:** Only updated with the processor, which guarantees the current values written in the IVIDx-I register.
2. **IVIDx-I:** Default set-up by the VR vendor and can be rewritten by the processor. The registers reflect the maximum instantaneous current for the phase number being defined.

The IVID registers must cooperate with registers MFR_1PHL and MFR_PHASE_HYS to determine the active phase number. Table 7 lists the operation condition and the phase number. Besides the basic rules listed in Table 7, the VR must also follow the same rules as listed in the auto-phase shedding function to improve the transient condition.

Figure 11 shows the IVID process, which takes the time set by register MFR_IVID_VALID_WAITTIME (F9h[15:8]) to start reducing the phase number after the VR is settled. Phase adding begins immediately after receiving the SetVID command.

Table 7: Phase Shedding and Adding Based on the VID

Condition		Phase Number
VID > IVID1 - VID		Full-phase CCM
IVIDx - VID ≥ VID > IVID (x + 1) - VID (x = 1, 2) or IVID3 - VID ≥ VID	$(n - 1) * MFR_1PHL < IVIDx - I \leq n * MFR_1PHL$ (n > 1)	N-phase CCM or full (<n) phase CCM
IVIDx - VID ≥ VID > IVID (x + 1) - VID (x = 1, 2) or IVID3 - VID ≥ VID	$5A < IVIDx - I \leq 1 * MFR_1PHL$	1-phase CCM
IVIDx - VID ≥ VID > IVID (x + 1) - VID (x = 1, 2) or IVID3 - VID ≥ VID	$IVIDx - I \leq 5A$	1-phase DCM

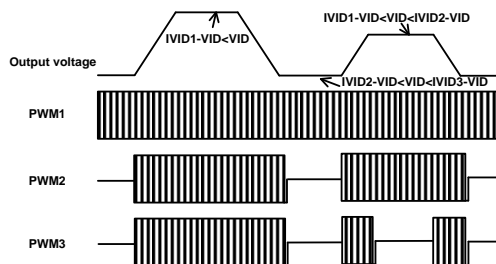


Figure 11: IVID Process during Voltage Change

When the auto-phase shedding and IVID functions are both enabled, the IVID function determines the phase number first according to Table 7 based on the VID. Then the VR begins phase shedding according to Table 6 based on the current report.

To set-up the auto-phase shedding and IVID functions, first set up the MFR_1PHL and MFR_PHASE_HYS according to the best efficiency performance of the Intelli-Phase. Then set up the IVID1-I, IVID2-I, and IVID3-I according to the load application.

PMBus and SVID Communication

The MP2949A supports real-time monitoring for the VR operation parameters and status with the PMBus and SVID interface (see Table 8).

Table 8: PMBus and SVID Monitored Parameters

Parameter	PMBus	SVID
Output voltage	✓	✓
Output current	✓	✓
Temperature	✓	✓
Input voltage	✓	✓
Input power	✓	✓
Phase current	✓	
OV	✓	
OC	✓	✓
UV	✓	
OT	✓	✓
CML	✓	

V_{IN} Protection

The MP2949A adopts a programmable V_{IN} protection with the following protection threshold programmed in the related PMBus registers.

- The VR will tri-state shut off immediately if the sensed input voltage is below VIN_OFF (36h[7:0]) and restarts when the sensed input voltage is above VIN_ON (35h[7:0]) with V_{IN} UVLO non-latch mode.
- The VR will latch if the sensed input voltage is above VIN_OV_FAULT_LIMIT (55h[7:0]) when V_{IN} OVP is set to latch mode.
- The VR is warned if the input voltage is below VIN_UV_WARNING_LIMIT (58h[7:0]).

Over-Voltage Protection (OVP)

The over-voltage protection (OVP) circuit monitors the output voltage for an over-voltage condition. The over-voltage signal generation is shown in Figure 12.

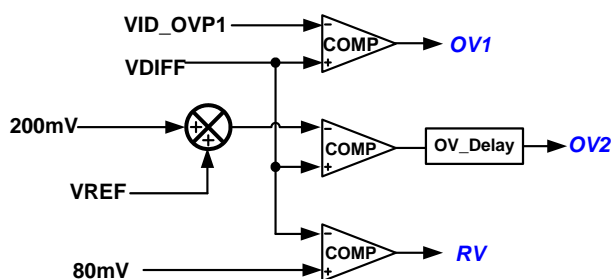


Figure 12: OVP and RVP Trigger Threshold

There are two levels of over-voltage protection.

The first level of over-voltage protection is OVP2. When the detected output voltage is 400mV higher than the reference voltage, the controller triggers OVP after a certain delay time. The OVP2 action latches PWM low to discharge the output until the output drops below 160mV, where reverse-voltage protection (RVP) is triggered. OVP2 can be defined as REF + 200mV for the 1/2 gain of output voltage to VDIFF. Figure 13 shows the VR behavior when OVP2 is triggered.

To avoid a false trigger, OVP2 is blanked during soft start and shutdown. The VID transition period includes SetVID_Fast/Slow/Decay, and sets PS4 as well.

The OVP2 default is latch off in normal IMVP8/9 applications. Other modes, like retry and hiccup mode, are available by setting the register

MFR_OVP_SET_MODE (F1h[3:2]). The OVP delay time is set by register OVP2 DELAYTIME (F7h[11:6]).

The second level of over-voltage protection is OVP1, which is set by MFR_FIXED_OVP_SET (F6h[6:0]). This is an absolute OV threshold, which is active whenever the controller is enabled, regardless of the operation or fault condition. In the event of an OVP1 condition, the PWMs are latched low to turn off the high-side MOSFETs (HS-FET) and turn on the low-side MOSFETs (LS-FET) to discharge the output voltage. The OVP1 latch can only be reset by toggling EN or VCC.

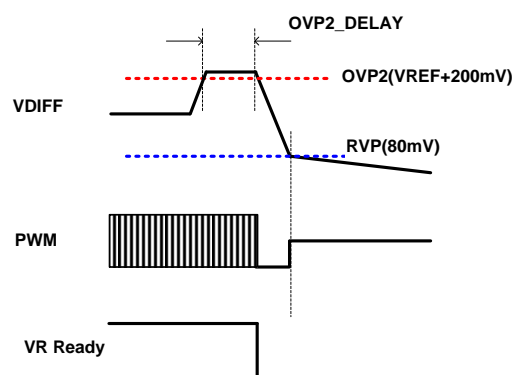


Figure 13: OVP and RVP Fault Protection

Reverse-Voltage Protection (RVP)

During OVP, the LS-FET remains on to drive the inductor current negative. A large reverse inductor current may produce negative output voltages that harm the processor and other output components. In addition to OVP, the MP2949A also implements an RVP function to avoid negative voltage ringing after the OV logic is triggered. Once VDIFF drops below 80mV, the MP2949A triggers RVP by latching all PWM outputs to tri-state. The reverse inductor current can reset to 0A quickly by dissipating the energy in the inductor to the input DC voltage source through the forward-biased body diode of the HS-FETs (see Figure 13).

Over-Current Protection (OCP)

The MP2949A provides a programmable total current protection in each rail to stop the VR from working at an extremely heavy load. This protection is triggered if the sensed average total output current is higher than the OC trigger level, MFR_OCP_SET_LEVEL (EEh[6:0]).

Once the sensed I_{OUT} is over the set over-current protection (OCP) level with a set delay time (MFR_OCP_SET_DELAYTIME (EEh[13:8])), the MP2949A turns off both the HS-FETs and LS-FETs by setting the PWM to tri-state (see Figure 14).

The total OCP limit and delay time are set at register EEh. Set the OCP set point at around $130\% \cdot I_{CCMAX}$. The OCP delay is recommended to be around 500 μ s.

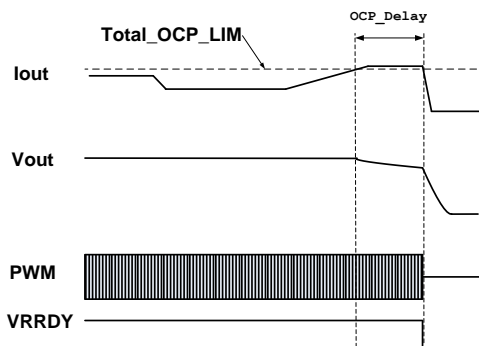


Figure 14: OCP for Total Current

Phase Current Limit Protection

In addition to the total over-current limit based on the sensed I_{OUT} , the MP2949A also utilizes a cycle-by-cycle valley point over-current limit method to limit each phase current. If the present phase current is higher than the setting valley point and remains for 80ns, this phase does not turn on, and the next phase turns on when its own PWM is on to regulate the output voltage at the set point. The phase current limit itself will not trigger a latch off. Latch off may occur when the phase current limit triggers either OCP or UVP.

The valley point over-current level can be programmed via the PMBus to limit per-phase current in register OCP_DA_LIMIT (EFh[15:8]).

Figure 15 shows the process when the output is shorted to ground. During this process, the per-phase OCP limits the phase current immediately, and the VR shuts down after a certain time.

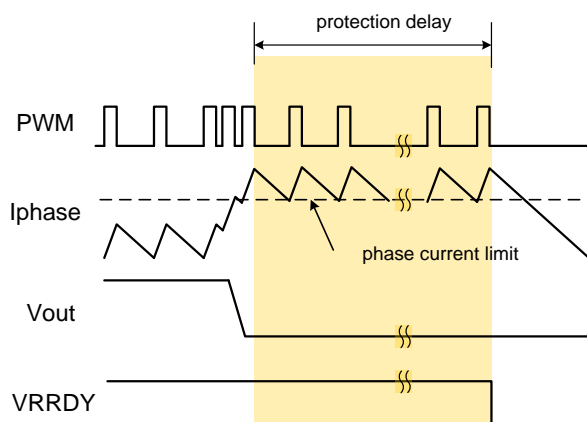


Figure 15: Phase Current Limit Protection during Output Dead Short

Under-Voltage Protection (UVP)

If the sensed output voltage (VDIFF) is below $V_{REF} - 150mV$ for a certain amount of time, the system triggers under-voltage protection (UVP), shuts down immediately, and turns off all phases by setting the PWM to tri-state (see Figure 16). Typically, UVP is triggered when OCP is reached. The UVP model (default latch) can be set through register MFR_UVP_SET_MODE (F1h[5:4]). The UVP delay time is set by register UVP_DELAYTIME (F7h[5:0]). See the Register Map section on page 71 and page 73 for more details.

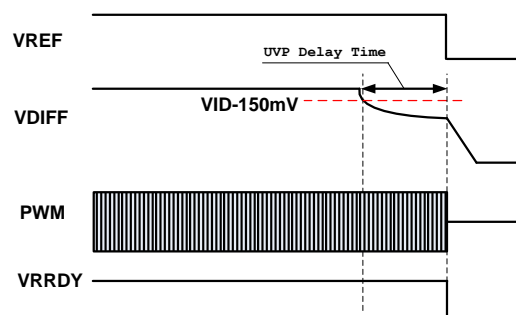


Figure 16: Under-Voltage Protection

VRHOT#

The VRHOT# fault is asserted when the sensed external temperature exceeds the maximum temperature threshold. This is used for fault reporting only and cannot shutdown the system. VRHOT# also has a fixed 3°C hysteresis when VRHOT# asserts when the sensed temperature exceeds the maximum temperature. VRHOT# also asserts when PSYS exceeds the critical value. VRHOT# is initialized in tri-state upon device power-up.

Phase Current Balancing/Thermal Balancing

The phase current to the MP2949A is sensed and calculated with the current reference in the slow current proportion integrate (PI) loop. Each phase's PWM on time is adjusted individually to balance the currents by applying Σ - Δ modulation and delay line loop technology in the current balance modulation, so the current is balanced, and the jitter is reduced greatly.

Each current balance loop can also include a programmable phase current offset to achieve thermal balance among the phases. The phase with the worse cooling capability can be set to receive less phase current by adding a offset on the CS sample value to keep the phase thermal balanced. See the Register Map section on page 70 for phase current offset configuration details.

SVID Interface

To support multiple VR devices used on the same SVID bus, the SVID address of each rail can be programmed independently through the register MFR_ADDR_SVID (E6h[11:0]). The SVID address is a 4-bit code for each rail. There are 14 addresses for up to 14 voltage regulator controllers or voltage rails. The final addresses (0Eh and 0Fh) are All Call addresses, and all VR controllers respond to these addresses.

The All Call address is only used with SetVID or SetPS commands. It cannot be used with GETreg or SetRegADR and SetRegDAT commands. The VR will NAK those commands with an All Call address. The VR acknowledges the All Call address in the same manner as a single address.

Input Power Sense

The SVID address 0Dh domain is defined to report system input power. When the voltage of PSYS reaches 0.8V, the platform input power reaches the maximum input power. The report value for the CPU is FFh in the SVID register 1Bh.

The input power sensing device sends out a current signal to the MP2949A proportional to the input power. A resistor from PSYS to GND converts the current into voltage. A bypass capacitor is also needed. Figure 17 shows the PSYS connection.

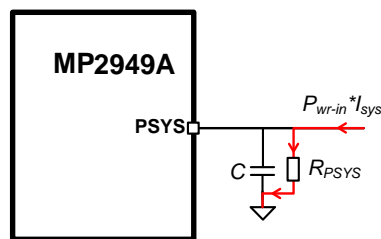


Figure 17: PSYS Connection

Calculate the PSYS resistor value with Equation (9):

$$R_{PSYS} = \frac{0.8}{P_{wr_in_max} \times I_{sys}} \quad (9)$$

Where I_{sys} is the current gain of the input power sensor (in $\mu A/W$), and $P_{wr_in_max}$ is the maximum input power (in W).

The averaging interval of input power sense is 1ms, and the register update interval is 500 μs .

PS4 Enter/Exit Mechanism

The target rail enters PS4 mode after receiving a SETPS4 command. The VR changes the VID of the rail to 00h and halts the PWM(s) of the rail immediately. ALT# is deasserted in PS4. Other rails maintain power conversion as normal. If all rails receive a SETPS4 command, the chip turns off PLL and disables as many analog circuits as possible to save power, except for the SVID interface with SLP_S0# deasserted (high).

The SetVID or SetPS0/1/2/3 command is used to wake up the VR from PS4 mode. Any rail that receives the SetVID or SetPS0/1/2/3 command enables the internal PLL and analog circuits. PS4 exits latency less than 90 μs counted from the acknowledgement of the PS4 exit command to where VID is ready to ramp (SETPS) or the start of ramping (SetVID).

SLP_S0# Signal Support

SLP_S0# is used to enable or disable the SVID interface when the VR is in PS4 mode. There is an enable bit, MFR_SLP_S0_FUN[0] (E6h[14]), that enables SLP_S0# assertion to disable the SVID interface when the VR is in PS4. The output voltage ramps down to 0V, and the IC turns most of the block off when it receives a SetPS4 command. To save more quiescent power, SLP_S0# is used to disable the SVID interface. When the system enters PS4 mode,

and SLP_S0# is asserted (low), the SVID interface (ALT#, SCLK, SDIO) is disabled. When SLP_S0# deasserts (high), the SVID interface becomes active. The output voltage remains at 0V and waits for the SetVID command to ramp up. If the VR is not in PS4, SLP_S0# assertion is blanked.

STB Function

STB is used to set the Intelli-Phase into standby mode by connecting STB to SYNC of the Intelli-Phase. In PS4 mode, STB enters tri-state, so the Intelli-Phase enters low-power mode to save power. In normal operation mode, STB is logic high. Figure 18 shows the connection between the MP2949A's STB pin and the Intelli-Phase's SYNC pin.

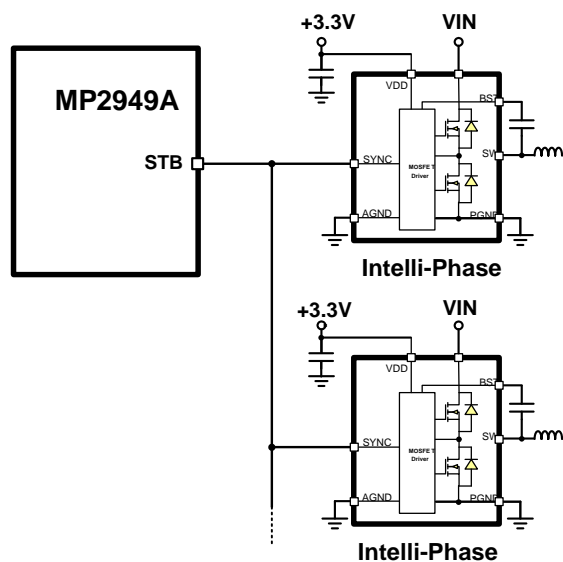


Figure 18: STB Connection between MP2949A and MPS Intelli-Phase

SVID Registers

Table 9 shows the data and configuration registers for the SVID protocol.

Table 9: SVID Data and Configuration Registers

Index	Register Name	Access	Default	Note
00h	Vendor ID	Read only by master, write by vendor	25h	Programmable through PMBus
01h	Product ID		0Bh	Programmable through PMBus
02h	Product revision		00h	Programmable through PMBus
05h	Protocol ID		05h	Programmable through PMBus
06h	Capability		81h	Programmable through PMBus
10h	Status_1	Read by master, write by PWM	00h	These registers are operation condition dependent. The register values vary with operating conditions.
11h	Status_2		00h	
12h	Temperature zone		00h	
15h	Output current (I _{OUT})		00h	
17h	VR temperature		00h	
1Bh	Input power		00h	
1Ch	Status2_last read		00h	
21h	ICC_MAX	Read only, configured by the platform	00h	Programmable through PMBus
24h	SR-fast		30mV/us	Programmable through PMBus
25h	SR-slow		15mV/us	Programmable through PMBus
30h	Vout max	Read and write by master	FFh	Can only be programmed by CPU
31h	VID setting		00H	Can only be programmed by CPU
32h	Pwr state		00H	Can only be programmed by CPU
34h	Multi VR configure	Read by master, write by PWM	01H	Programmable through PMBus
42h	IVID1-VID	Read and write by master	00h	Programmable through PMBus
44h	IVID2-VID		00h	Programmable through PMBus
46h	IVID3-VID		00h	Programmable through PMBus
43h	IVID1-I		0Fh	CPU may program these registers during system boot
45h	IVID2-I		0Fh	
47h	IVID3-I		05h	

VID Range

The MP2949A covers the full IMVP8/IMVP9 VID range. The IMVP8 VID is 0V, 0.25V ~ 1.52V. In the range of 0.25V ~ 1.52V, the voltage step is 5mV/step. The IMVP9 VID step could be 5mV and 10mV. The voltage of the 5mV VID step is the same as IMVP8. The 10mV/step of IMVP9 VID is 0V, 0.2V ~ 2.74V. In the range of 0.2V ~ 2.74V, the voltage step is 10mV/step (see Table 10 and Table 11).

Table 10: IMVP8/IMVP9 5mV VID Step VID Table

VID (HEX)	V _{OUT} (V)	VID (HEX)	V _{OUT} (V)	VID (HEX)	V _{OUT} (V)	VID (HEX)	V _{OUT} (V)
00	0	40	0.565	80	0.885	C0	1.205
01	0.25	41	0.57	81	0.89	C1	1.21
02	0.255	42	0.575	82	0.895	C2	1.215
03	0.26	43	0.58	83	0.9	C3	1.22
04	0.265	44	0.585	84	0.905	C4	1.225
05	0.27	45	0.59	85	0.91	C5	1.23
06	0.275	46	0.595	86	0.915	C6	1.235
07	0.28	47	0.6	87	0.92	C7	1.24
08	0.285	48	0.605	88	0.925	C8	1.245
09	0.29	49	0.61	89	0.93	C9	1.25
0A	0.295	4A	0.615	8A	0.935	CA	1.255
0B	0.3	4B	0.62	8B	0.94	CB	1.26
0C	0.305	4C	0.625	8C	0.945	CC	1.265
0D	0.31	4D	0.63	8D	0.95	CD	1.27
0E	0.315	4E	0.635	8E	0.955	CE	1.275
0F	0.32	4F	0.64	8F	0.96	CF	1.28
10	0.325	50	0.645	90	0.965	D0	1.285
11	0.33	51	0.65	91	0.97	D1	1.29
12	0.335	52	0.655	92	0.975	D2	1.295
13	0.34	53	0.66	93	0.98	D3	1.3
14	0.345	54	0.665	94	0.985	D4	1.305
15	0.35	55	0.67	95	0.99	D5	1.31
16	0.355	56	0.675	96	0.995	D6	1.315
17	0.36	57	0.68	97	1	D7	1.32
18	0.365	58	0.685	98	1.005	D8	1.325
19	0.37	59	0.69	99	1.01	D9	1.33
1A	0.375	5A	0.695	9A	1.015	DA	1.335
1B	0.38	5B	0.7	9B	1.02	DB	1.34
1C	0.385	5C	0.705	9C	1.025	DC	1.345
1D	0.39	5D	0.71	9D	1.03	DD	1.35
1E	0.395	5E	0.715	9E	1.035	DE	1.355
1F	0.4	5F	0.72	9F	1.04	DF	1.36
20	0.405	60	0.725	A0	1.045	E0	1.365
21	0.41	61	0.73	A1	1.05	E1	1.37
22	0.415	62	0.735	A2	1.055	E2	1.375
23	0.42	63	0.74	A3	1.06	E3	1.38
24	0.425	64	0.745	A4	1.065	E4	1.385
25	0.43	65	0.75	A5	1.07	E5	1.39
26	0.435	66	0.755	A6	1.075	E6	1.395
27	0.44	67	0.76	A7	1.08	E7	1.4
28	0.445	68	0.765	A8	1.085	E8	1.405
29	0.45	69	0.77	A9	1.09	E9	1.41
2A	0.455	6A	0.775	AA	1.095	EA	1.415
2B	0.46	6B	0.78	AB	1.1	EB	1.42
2C	0.465	6C	0.785	AC	1.105	EC	1.425
2D	0.47	6D	0.79	AD	1.11	ED	1.43
2E	0.475	6E	0.795	AE	1.115	EE	1.435
2F	0.48	6F	0.8	AF	1.12	EF	1.44
30	0.485	70	0.805	B0	1.125	F0	1.445
31	0.49	71	0.81	B1	1.13	F1	1.45
32	0.495	72	0.815	B2	1.135	F2	1.455
33	0.5	73	0.82	B3	1.14	F3	1.46
34	0.505	74	0.825	B4	1.145	F4	1.465
35	0.51	75	0.83	B5	1.15	F5	1.47
36	0.515	76	0.835	B6	1.155	F6	1.475
37	0.52	77	0.84	B7	1.16	F7	1.48
38	0.525	78	0.845	B8	1.165	F8	1.485
39	0.53	79	0.85	B9	1.17	F9	1.49
3A	0.535	7A	0.855	BA	1.175	FA	1.495
3B	0.54	7B	0.86	BB	1.18	FB	1.5
3C	0.545	7C	0.865	BC	1.185	FC	1.505
3D	0.55	7D	0.87	BD	1.19	FD	1.51
3E	0.555	7E	0.875	BE	1.195	FE	1.515
3F	0.56	7F	0.88	BF	1.2	FF	1.52

Table 11: IMVP9 10mV VID Step VID Table

VID (HEX)	V _{OUT} (V)	VID (HEX)	V _{OUT} (V)	VID (HEX)	V _{OUT} (V)	VID (HEX)	V _{OUT} (V)
00	0	40	0.83	80	1.47	C0	2.11
01	0.2	41	0.84	81	1.48	C1	2.12
02	0.21	42	0.85	82	1.49	C2	2.13
03	0.22	43	0.86	83	1.5	C3	2.14
04	0.23	44	0.87	84	1.51	C4	2.15
05	0.24	45	0.88	85	1.52	C5	2.16
06	0.25	46	0.89	86	1.53	C6	2.17
07	0.26	47	0.9	87	1.54	C7	2.18
08	0.27	48	0.91	88	1.55	C8	2.19
09	0.28	49	0.92	89	1.56	C9	2.2
0A	0.29	4A	0.93	8A	1.57	CA	2.21
0B	0.3	4B	0.94	8B	1.58	CB	2.22
0C	0.31	4C	0.95	8C	1.59	CC	2.23
0D	0.32	4D	0.96	8D	1.6	CD	2.24
0E	0.33	4E	0.97	8E	1.61	CE	2.25
0F	0.34	4F	0.98	8F	1.62	CF	2.26
10	0.35	50	0.99	90	1.63	D0	2.27
11	0.36	51	1	91	1.64	D1	2.28
12	0.37	52	1.01	92	1.65	D2	2.29
13	0.38	53	1.02	93	1.66	D3	2.3
14	0.39	54	1.03	94	1.67	D4	2.31
15	0.4	55	1.04	95	1.68	D5	2.32
16	0.41	56	1.05	96	1.69	D6	2.33
17	0.42	57	1.06	97	1.7	D7	2.34
18	0.43	58	1.07	98	1.71	D8	2.35
19	0.44	59	1.08	99	1.72	D9	2.36
1A	0.45	5A	1.09	9A	1.73	DA	2.37
1B	0.46	5B	1.1	9B	1.74	DB	2.38
1C	0.47	5C	1.11	9C	1.75	DC	2.39
1D	0.48	5D	1.12	9D	1.76	DD	2.4
1E	0.49	5E	1.13	9E	1.77	DE	2.41
1F	0.5	5F	1.14	9F	1.78	DF	2.42
20	0.51	60	1.15	A0	1.79	E0	2.43
21	0.52	61	1.16	A1	1.8	E1	2.44
22	0.53	62	1.17	A2	1.81	E2	2.45
23	0.54	63	1.18	A3	1.82	E3	2.46
24	0.55	64	1.19	A4	1.83	E4	2.47
25	0.56	65	1.2	A5	1.84	E5	2.48
26	0.57	66	1.21	A6	1.85	E6	2.49
27	0.58	67	1.22	A7	1.86	E7	2.5
28	0.59	68	1.23	A8	1.87	E8	2.51
29	0.6	69	1.24	A9	1.88	E9	2.52
2A	0.61	6A	1.25	AA	1.89	EA	2.53
2B	0.62	6B	1.26	AB	1.9	EB	2.54
2C	0.63	6C	1.27	AC	1.91	EC	2.55
2D	0.64	6D	1.28	AD	1.92	ED	2.56
2E	0.65	6E	1.29	AE	1.93	EE	2.57
2F	0.66	6F	1.3	AF	1.94	EF	2.58
30	0.67	70	1.31	B0	1.95	F0	2.59
31	0.68	71	1.32	B1	1.96	F1	2.6
32	0.69	72	1.33	B2	1.97	F2	2.61
33	0.7	73	1.34	B3	1.98	F3	2.62
34	0.71	74	1.35	B4	1.99	F4	2.63
35	0.72	75	1.36	B5	2	F5	2.64
36	0.73	76	1.37	B6	2.01	F6	2.65
37	0.74	77	1.38	B7	2.02	F7	2.66
38	0.75	78	1.39	B8	2.03	F8	2.67
39	0.76	79	1.4	B9	2.04	F9	2.68
3A	0.77	7A	1.41	BA	2.05	FA	2.69
3B	0.78	7B	1.42	BB	2.06	FB	2.7
3C	0.79	7C	1.43	BC	2.07	FC	2.71
3D	0.8	7D	1.44	BD	2.08	FD	2.72
3E	0.81	7E	1.45	BE	2.09	FE	2.73
3F	0.82	7F	1.46	BF	2.1	FF	2.74

Selected PMBus Register Map

The PMBus registers are distributed into three pages: Page 0, Page 1, and Page 2. Page 0 contains the registers for Rail A and most of the common settings for all of the rails. Page 1 contains register information for Rail B. Page 2 contains register information for Rail C. This section contains most of the functional registers for all of the rails with details on how to program the register data.

PMBUS COMMANDS/REGISTERS RAIL A/B/C (PAGE 0/1/2)

Command Code	Command Name	Type	Bytes	Page 0	Page 1	Page 2
00h	PAGE	r/w	1	✓	✓	✓
01h	OPERATION	r/w	1	✓	✓	✓
03h	CLEAR_FAULTS	send	0	✓	✓	✓
07h	LAST_FAULT_BLOCK	r/w	2	✓		
08h	CLEAR_LAST_FAULT	send	0	✓	✓	✓
15h	STORE_USER_ALL	send	0	✓	✓	✓
16h	RESTORE_USER_ALL	send	0	✓	✓	✓
1Bh	IDROOP_CTRL	r/w	2	✓	✓	
1Dh	MFR_EEPROM_CTRL	r/w	2	✓		
1Eh	PSYS_WARN_FILT_CNT	r/w	1	✓		
21h	VOUT_COMMAND	r/w	2	✓	✓	✓
22h	MFR_VOUT_TRIM	r/w	2	✓	✓	✓
23h	VOUT_CAL_OFFSET	r/w	2	✓	✓	✓
24h	MFR_VOUT_MAX	r/w	2	✓	✓	✓
25h	VOUT_MARGIN_HIGH	r/w	2	✓	✓	✓
26h	VOUT_MARGIN_LOW	r/w	2	✓	✓	✓
2Bh	MFR_IMMEDIATE_SET	r/w	2	✓	✓	✓
2Ch	SNS_PICK	r/w	2	✓		
2Dh	MFR_ADC_SET	r/w	2	✓		
2Eh	MFR_PROTECT_CFG	r/w	2	✓		
2Fh	MFR_DEBUG	r/w	2	✓	✓	✓
35h	VIN_ON	r/w	2	✓		
36h	VIN_OFF	r/w	2	✓		
38h	IOUT_CAL_GAIN	r/w	2	✓	✓	✓
39h	IOUT_CAL_OFFSET	r/w	2	✓	✓	✓
55h	VIN_OV_FAULT_LIMIT	r/w	2	✓		
58h	VIN_UV_WARNING_LIMIT	r/w	2	✓		
72h	SVID_REG_80H_81H	r	2	✓		
73h	SVID_REG_82H	r	1	✓		
74h	SLAVE_ADDR	r	1	✓		
75h	MFR_CS_1_2	r	2	✓		
76h	MFR_CS_3_4	r	2	✓		
77h	MFR_CS_5_6	r	2	✓		
7Ah	STATUS_VOUT	r	1	✓	✓	✓
7Bh	STATUS_IOUT	r	1	✓	✓	✓
7Ch	STATUS_INPUT	r	1	✓		
88h	READ_VIN	r	2	✓		
8Bh	READ_VOUT	r	2	✓	✓	✓
8Ch	READ_IOUT	r	2	✓	✓	✓
8Dh	READ_TEMPERATURE	r	2	✓		
96h	READ_POUT	r	2	✓	✓	✓
97h	READ_PIN	r	2	✓		
B8h	MFR_VIN_HYS	r/w	1	✓		
BBh	MFR_1PHL	r/w	1	✓		
BCh	MFR_PHASE_HYS	r/w	1	✓		
BDh	PROTOCOL_ID_RD_RC_TA, ENABLE_TO_SVID_RDY_VR	r/w	2	✓		
BEh	PS3_PS4_EXIT_DELAY	r/w	2	✓	✓	✓
BFh	VENDOR_ID_PRODUCT_ID	r/w	2	✓		

PMBUS COMMANDS/REGISTERS RAIL A/B/C (PAGE 0/1/2) (continued)

Command Code	Command Name	Type	Bytes	Page0	Page1	Page2
C0h	PRODUCT_REV_DATA	r/w	2	✓		
C1h	CODE_REV_PROTOCOL_RB_RA	r/w	2	✓		
C2h	DECAY_CFG_34H_06H	r/w	2	✓	✓	✓
C3h	TOLERANCE_SR_FAST	r/w	2	✓	✓	✓
C4h	MFR_VOUT_MAX_9BIT	r/w	2	✓	✓	✓
C5h	IVID2_1_I_DEF	r/w	2	✓	✓	✓
C6h	PIN_MAX_IVID3_I_DEF	r/w	2	✓	✓	✓
CAh	MFR_PHASE_CFG	r/w	1	✓		
CBh	T_DC_DROPPH_V_LOWFS	r/w	2	✓		
CCh	DC_CTRL_ADAP_CTRL	r/w	2	✓	✓	✓
CDh	HF_PFM_SLP_DISCHG	r/w	2	✓	✓	✓
Ceh	MINOFF_BLANK_TIME	r/w	2	✓		
CFh	MFR_PFM_SET	r/w	2	✓		
D0h	MFR_SLOPE_SR_6P	r/w	2	✓		
D1h	MFR_SLOPE_CNT_6P	r/w	2	✓		
D2h	MFR_SLOPE_SR_5P	r/w	2	✓		
D3h	MFR_SLOPE_CNT_5P	r/w	2	✓		
D4h	MFR_SLOPE_SR_4P	r/w	2	✓		
D5h	MFR_SLOPE_CNT_4P	r/w	2	✓		
D6h	MFR_SLOPE_SR_3P	r/w	2	✓		
D7h	MFR_SLOPE_CNT_3P	r/w	2	✓		
D8h	MFR_SLOPE_SR_2P	r/w	2	✓		
D9h	MFR_SLOPE_CNT_2P	r/w	2	✓		
Dah	MFR_SLOPE_SR_1P	r/w	2	✓		
DBh	MFR_SLOPE_CNT_1P	r/w	2	✓		
DCh	MFR_SLOPE_SR_DCM	r/w	2	✓		
DDh	MFR_SLOPE_CNT_DCM	r/w	2	✓		
Deh	MFR_TRIM_2_1_DCM	r/w	2	✓	✓	✓
DFh	MFR_TRIM_5_4_3	r/w	2	✓		
E0h	MFR_TRIM_6	r/w	1	✓		
E1h	SHUTLEVEL_ADDRPMBUS	r/w	2	✓		
E2h	MFR_CB_SATU_PI	r/w	2	✓	✓	
E3h	VTRIM_STEP_VCAL_PI	r/w	2	✓	✓	✓
E4h	MFR_VR_CONFIG	r/w	2	✓	✓	✓
E5h	MFR_FS_VBOOT	r/w	2	✓	✓	✓
E6h	MFR_ADDR_SVID	r/w	2	✓		
E7h	VFB_TRIM_DCLL	r/w	2	✓	✓	✓
E8h	TEMPERATURE_GAIN_OFFSET	r/w	2	✓		
E9h	MFR_CUR_GAIN	r/w	2	✓	✓	✓
EAh	MFR_CUR_OFFSET	r/w	1	✓	✓	✓
EBh	MFR_CS_OFFSET1_2	r/w	2	✓		
ECh	MFR_CS_OFFSET3_4	r/w	2	✓		
EDh	MFR_CS_OFFSET5_6	r/w	2	✓		
EEh	MFR_OCP_SET_LEVEL	r/w	2	✓	✓	✓
EFh	OC_LIMIT_ICC_MAX	r/w	2	✓	✓	✓



PMBUS COMMANDS/REGISTERS RAIL A/B/C (PAGE 0/1/2) (continued)

Command Code	Command Name	Type	Bytes	Page0	Page1	Page2
F0h	MFR_VOUT_CMPS_MAX	r/w	1	✓		
F1h	UVP_OVP_OCP_MODE	r/w	2	✓	✓	✓
F2h	MFR_OTP_SET	r/w	2	✓		
F3h	MFR_TEMP_MAX	r/w	1	✓		
F6h	MFR_FIXED_OVP_SET	r/w	1	✓	✓	✓
F7h	MFR_OVP_UVP_SET	r/w	2	✓		
F9h	MFR_FILTER_SET	r/w	2	✓	✓	✓
FAh	MFR_TRANS_FAST	r/w	2	✓	✓	✓
FBh	MFR_EN_DLY	r/w	2	✓	✓	✓
FCh	MFR_IMON_SVID	r/w	2	✓	✓	✓
FDh	MFR_ALT_SET	r/w	2	✓	✓	✓
FEh	CLEAR_EEPROM_FAULTS	send	0	✓	✓	✓



PAGE 0 REGISTER MAP

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor through only one physical address for the three rails and test mode.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w
Function	X	X	X	X	X	X	PAGE	

Bits	Bit Name	Description
[7:2]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[1:0]	PAGE	2'b00: Page 0, all commands address Rail A 2'b01: Page 1, all commands address Rail B 2'b10: Page 2, all commands address Rail C Others: ineffective input

OPERATION (01h)

The OPERATION command on Page 0 is used to turn the Rail A output on or off in conjunction with input from EN. OPERATION is also used to set the output voltage to the upper or lower margin voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of EN instructs the device to change to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OPERATION_MODE							

Bits	Bit Name	Description
[7:0]	OPERATION_MODE	Sets the operation mode for Rail A. 7'b00xxxxx: immediate off 7'b1000xxxx: normal on 7'b1001xxxx: margin low 7'b1010xxxx: margin high 7'b100101xx: margin low, ignore fault (ignore UV) 7'b101001xx: margin high, ignore fault (ignore OV2) The value of "x" does not matter.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set on Rail A. This command clears all bits in all status registers simultaneously. This command is write only. There is no data byte for this command.

LAST_FAULT_BLOCK (07h)

This command is used to record any protection, regardless of the rail when OVP1, OVP2, OCP, UVP, VIN_OVP, VIN_UVLO, OTP, or TEMP_FAULT occurs.

Command	LAST_FAULT_BLOCK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function																

Bits	Bit Name	Description
[15]	OVP1_RailC	Flag of Rail C OVP1. Read only.
[14]	OVP2_RailC	Flag of Rail C OVP2. Read only.
[13]	OCP_RailC	Flag of Rail C OCP. Read only.
[12]	UVP_RailC	Flag of Rail C UVP. Read only.
[11]	OVP1_RailB	Flag of Rail B OVP1. Read only.
[10]	OVP2_RailB	Flag of Rail B OVP2. Read only.
[9]	OCP_RailB	Flag of Rail B OCP. Read only.
[8]	UVP_RailB	Flag of Rail B UVP. Read only.
[7]	OVP1_RailA	Flag of Rail A OVP1. Read only.
[6]	OVP2_RailA	Flag of Rail A OVP2. Read only.
[5]	OCP_RailA	Flag of Rail A OCP. Read only.
[4]	UVP_RailA	Flag of Rail A UVP. Read only.
[3]	VIN_OVP	Flag of VIN OVP. Read only.
[2]	VIN_UVLO	Flag of VIN UVLO. Read only.
[1]	OTP	Flag of OTP. Read only.
[0]	TEMP_FAULT	Flag of TEMP fault. Read only.

When VR restarts after a protection shutdown, the data of the flag in MTP is restored to memory 07h. If any bit of 07h is 1'b1, protect_fault_record_en = 1, and register 1Dh[6] is equal to 1'b1, the VR will not start up after sending the CLEAR_EEPROM_FAULTS (FEh) command until the CLEAR_LAST_FAULT command (08h) is sent.

CLEAR_LAST_FAULT (08h)

See the LAST_FAULT_BLOCK (07h) section above.

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus device to copy the Page 0 ~ Page 2 contents (not including read-only registers) of the operating memory to the matching locations in the MTP, regardless of the current PMBus register page. This command can be used while the device is outputting power. This command is write only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBus device to copy the Page 0 ~ Page 2 contents of the MTP to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the user store. Any items in the user store that do not have matching locations in the operating memory are ignored. It is *not* permitted to use this command while the device is outputting power unless MFR_EEPROM_COPY_EN (register 1Dh[1] on Page 0) is set to 1. This command is write only. There is no data byte for this command.

IDROOP_CTRL (1Bh)

The IDROOP_CTRL command on Page 0 is used to set the IDROOP bandwidth for all rails and the IDROOP DC gain for Rail A.

Command	IDROOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	IDROOP_BW_EN			X		IDROOP_DC_SET			

Bits	Bit Name	Description																																				
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.																																				
[8:6]	IDROOP_BW_EN	Bit[8]: sets the IDROOP bandwidth of Rail A Bit[7]: sets the IDROOP bandwidth of Rail B Bit[6]: sets the IDROOP bandwidth of Rail C 1'b0: 8.5kHz, low bandwidth 1'b1: 12.5kHz, high bandwidth																																				
[5]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.																																				
[4]	IDROOP_EN	Selection bit of the AC droop of Rail A. 1'b0: enable DC droop 1'b1: enable AC droop																																				
[3:0]	IDROOP_DC_SET	Sets the IDROOP DC gain to set the digital load line gain. The default value of 'Idroop_set' is 1 h.																																				
		<table><tr><th>Idroop_set[3:0]</th><th>Gain</th><th>Idroop_set[3:0]</th><th>Gain</th></tr><tr><td>0 h</td><td>0</td><td>8 h</td><td>11/8 * 1/8</td></tr><tr><td>1 h</td><td>4/8 * 1/8</td><td>9 h</td><td>12/8 * 1/8</td></tr><tr><td>2 h</td><td>5/8 * 1/8</td><td>A h</td><td>13/8 * 1/8</td></tr><tr><td>3 h</td><td>6/8 * 1/8</td><td>B h</td><td>14/8 * 1/8</td></tr><tr><td>4 h</td><td>7/8 * 1/8</td><td>C h</td><td>15/8 * 1/8</td></tr><tr><td>5 h</td><td>8/8 * 1/8</td><td>D h</td><td>16/8 * 1/8</td></tr><tr><td>6 h</td><td>9/8 * 1/8</td><td>E h</td><td>17/8 * 1/8</td></tr><tr><td>7 h</td><td>10/8 * 1/8</td><td>F h</td><td>18/8 * 1/8</td></tr></table>	Idroop_set[3:0]	Gain	Idroop_set[3:0]	Gain	0 h	0	8 h	11/8 * 1/8	1 h	4/8 * 1/8	9 h	12/8 * 1/8	2 h	5/8 * 1/8	A h	13/8 * 1/8	3 h	6/8 * 1/8	B h	14/8 * 1/8	4 h	7/8 * 1/8	C h	15/8 * 1/8	5 h	8/8 * 1/8	D h	16/8 * 1/8	6 h	9/8 * 1/8	E h	17/8 * 1/8	7 h	10/8 * 1/8	F h	18/8 * 1/8
		Idroop_set[3:0]	Gain	Idroop_set[3:0]	Gain																																	
		0 h	0	8 h	11/8 * 1/8																																	
		1 h	4/8 * 1/8	9 h	12/8 * 1/8																																	
		2 h	5/8 * 1/8	A h	13/8 * 1/8																																	
		3 h	6/8 * 1/8	B h	14/8 * 1/8																																	
		4 h	7/8 * 1/8	C h	15/8 * 1/8																																	
		5 h	8/8 * 1/8	D h	16/8 * 1/8																																	
6 h	9/8 * 1/8	E h	17/8 * 1/8																																			
7 h	10/8 * 1/8	F h	18/8 * 1/8																																			

MFR_EEPROM_CTRL (1Dh)

The MFR_EEPROM_CTRL command on Page 0 is used to disable the gate clocks and control the operation of the MTP and LAST_FAULT_BLOCK function.

Command	MFR_EEPROM_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r	r	r/w	r/w	r/w	r/w
Function											X	X				

Bits	Bit Name	Description
[15]	gateclk_svid_sync_dis	Disables gateclk_svid_sync, active high. 1'b0: enable. Clock of SVID signal synchronization appears when needed. Can save power dissipation. 1'b1: disable. Clock of SVID signal synchronization always appears.
[14]	gateclk_pwm_sub_dis	Disables gateclk_pwm_sub, high effective (see above "gateclk_svid_sync_dis").
[13]	gateclk_cal_dis	Disables gateclk_cal, high effective (see above "gateclk_svid_sync_dis").
[12]	gateclk_opr_dis	Disables gateclk_opr, high effective (see above "gateclk_svid_sync_dis").
[11]	gateclk_ana_dis	Disables gateclk_ana, high effective (see above "gateclk_svid_sync_dis").
[10]	gateclk_mem_dis	Disables gateclk_mem, high effective (see above "gateclk_svid_sync_dis").
[9]	gateclk_reg_dis	Disables gateclk_reg, high effective (see above "gateclk_svid_sync_dis").
[8]	gateclk_reg_slave_dis	Disables gateclk_reg_slave, high effective (see above "gateclk_svid_sync_dis").
[7]	reg_1dh_b7	Enable bit to clear memory 07h after the CLEAR_LAST_FAULT command takes effect. 1'b0: disable 1'b1: enable
[6]	reg_1dh_b6	Enable bit to block start-up if a protection occurred during the last operating cycle. 1'b0: disable 1'b1: enable
[5:4]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[3]	clr_eeeprom_last_fault_en	Enable bit of the CLEAR_LAST_FAULT command (08h). 1'b0: disable 1'b1: enable
[2]	protect_fault_record_en	Enable bit to record protection information into MTP. 1'b0: disable 1'b1: enable when protection occurs. VR records protection information into MTP automatically
[1]	MFR_EEPROM_COPY_EN	Enable bit to read (restore) MTP while outputting power. 1'b0: disable 1'b1: enable
[0]	MFR_CRC_PROTECT_EN	Enable bit of CRC protect. 1'b0: disable 1'b1: enable

PSYS_WARN_FILT_CNT (1Eh)

The PSYS_WARN_FILT_CNT command on Page 0 is used to set the filter time of PSYS.

Command	PSYS_WARN_FILT_CNT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w
Function	X	X	X	X	X	PSYS_WARN_FILT_CNT		

Bits	Bit Name	Description
[7:3]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[2:0]	PSYS_WARN_FILT_CNT	Used to set the filter time of psys_warn2 and psys_warn1. If [2:0] = 0, use the ordinary 2-level FF synchronization, or the psys_warn2/1 positive edge delays ([2:1] + 1)*100ns, and a negative edge delays 100ns based on the 2FFs sync.

VOUT_COMMAND (21h)

The VOUT_COMMAND command on Page 0 sets the Rail A output voltage when the PMBus controls the output.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_COMMAND							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VOUT_COMMAND	Set the Rail A reference voltage (VID_DAC output voltage) in PMBus mode. In 5mV mode (E4h[5] = 1'b1): $V_{REF} = (VID + 49) / 2 * 5mV$ In 10mV mode (E4h[5] = 1'b0): $V_{REF} = (VID + 19) / 2 * 10mV$

MFR_VOUT_TRIM (22h)

This MFR_VOUT_TRIM command on Page 0 is used to apply a fixed offset voltage to the Rail A output voltage command value for different power states. This command is most typically used by the end user to trim the output voltage at the time the PMBus device is assembled into the end user's system.

Command	MFR_VOUT_TRIM															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VOUT_TRIM_3_6_CCM				VOUT_TRIM_2_CCM				VOUT_TRIM_1_CCM				VOUT_TRIM_1_DCM			

Bits	Bit Name	Description
[15:12]	VOUT_TRIM_3_6_CCM	Applies a fixed offset voltage to the Rail A output voltage at 3- to 6-phase CCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.
[11:8]	VOUT_TRIM_2_CCM	Applies a fixed offset voltage to the Rail A output voltage at 2-phase CCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.
[7:4]	VOUT_TRIM_1_CCM	Applies a fixed offset voltage to the Rail A output voltage at 1-phase CCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.
[3:0]	VOUT_TRIM_1_DCM	Applies a fixed offset voltage to the Rail A output voltage at 1-phase DCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.

VOUT_CAL_OFFSET (23h)

The VOUT_CAL_OFFSET command on Page 0 offers an offset VID to the Rail A target determined by VOUT_COMMAND, VOUT_MARGIN_HIGH, and VOUT_MARGIN_LOW. This command is the initial value of the Rail A SVID offset.

Command	VOUT_CAL_OFFSET															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_CAL_OFFSET							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VOUT_CAL_OFFSET	Sets the VID offset in PMBus mode. It is also the initial value for the SVID offset register (33h). 5mV/LSB or 10mV/LSB according to E4h[5], -80h ~ +7Fh.

MFR_VOUT_MAX (24h)

The MFR_VOUT_MAX command on Page 0 is the Rail A initial value of SVID VOUT_MAX (SVID 30h), which sets an upper limit on the VID target (not including the offset) of SVID to provide a safeguard against an accidental setting of the output voltage to a possibly destructive level. If an attempt is made to program the VID target higher than VOUT_MAX, the command is rejected. The PMBus VID target is not constrained by MFR_VOUT_MAX.

Command	MFR_VOUT_MAX															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	MFR_VOUT_MAX							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	MFR_VOUT_MAX	Sets an upper limit on the Rail A VID target (not including the offset) of SVID.

VOUT_MARGIN_HIGH (25h)

The VOUT_ATOM_SLP_DEAST command on Page 0 is used to set the Rail A VID target when the SLP_S0# signal de-asserts on the ATOM platform. The VOUT_MARGIN_HIGH command is used to set the Rail A reference voltage (VID_DAC output voltage) at the command MARGIN HIGH state.

Command	VOUT_MARGIN_HIGH															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VOUT_ATOM_SLP_DEAST								VOUT_MARGIN_HIGH							

Bits	Bit Name	Description
[15:8]	VOUT_ATOM_SLP_DEAST	Sets the Rail A reference voltage (VID_DAC output voltage) when SLP_S0# asserts in ATOM mode.
[7:0]	VOUT_MARGIN_HIGH	Sets the Rail A reference voltage (VID_DAC output voltage) at the command MARGIN HIGH state.

VOUT_MARGIN_LOW (26h)

The VOUT_ATOM_SLP_AST command on Page 0 is used to set the Rail A VID target when the SLP_S0# signal asserts on the ATOM platform. The VOUT_MARGIN_LOW command is used to set the Rail A reference voltage (VID_DAC output voltage) at the command MARGIN LOW state.

Command	VOUT_MARGIN_LOW															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VOUT_ATOM_SLP_AST								VOUT_MARGIN_LOW							

Bits	Bit Name	Description
[15:8]	VOUT_ATOM_SLP_AST	Sets the Rail A reference voltage (VID_DAC output voltage) when SLP_S0# de-asserts in ATOM mode.
[7:0]	VOUT_MARGIN_LOW	Sets the Rail A reference voltage (VID_DAC output voltage) at the command MARGIN LOW state.

MFR_IMMEDIATE_SET (2Bh)

The MFR_IMMEDIATE_SET command on Page 0 sets the Rail A slew rate, alert time, and bit[0] of STATUS1 when SVID sends VID within ± 2 LSB in 5mV mode.

Command	MFR_IMMEDIATE_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:8]	MFR_IMMED_REF_STEP	Sets the VID (output reference) step when SVID sends VID within ± 2 LSB in 5mV mode of Rail A.
[7:5]	MFR_IMMED_ALT_TIME	Sets the time length of the ALTER slewing one step (FD[13:12] + 1) when SVID sends VID within ± 2 LSB in 5mV mode of Rail A. 100ns/LSB.
[4:2]	MFR_IMMED_REF_TIME	Sets the time length of the VID slewing one step ([9:8]) when the SVID sends VID within ± 2 LSB in 5mV mode of Rail A. 100ns/LSB.
[1]	MFR_IMMEDIATE_SVID_EN	Enable bit of Rail A to force the STATUS bit[0] to 1'b1. 1'b0: disable. STATUS bit[0] remains at 1'b0 until it settles normally. 1'b1: enable. Forces STATUS bit[0] to 1'b1 when the SetVID command is received within ± 2 LSB.
[0]	MFR_IMMEDIATE_REF_EN	Enable bit of Rail A using bit[9:2]. 1'b0: disable 1'b1: enable

SNS_PICK (2Ch)

The SNS_PICK command monitors the ADC sense values and other internal signals and temp_cmp_sync10mhz. temp_cmp_sync10mhz is the sync result of the analog temperature fault (Intelli-Phase OC fault) signal.

Command	SNS_PICK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	SNS_PICK_CFG						SNS_PICK									

Bits	Bit Name	Description
[15:11]	SNS_PICK_CFG	Points to the appropriate register value.
[10]	temp_cmp_sync10mhz	Sync result of the analog temperature fault (Intelli-Phase OC fault) signal.
[9:0]	SNS_PICK	SNS_PICK_CFGSNS_PICK 5'h00 Current of phase 1 5'h01 Current of phase 2 5'h02 Current of phase 3 5'h03 Current of phase 4 5'h04 Current of phase 5 5'h05 Current of phase 6 5'h06 Input voltage 5'h07 VFB of Rail A 5'h08 VDIFF of Rail A 5'h09 IMONA voltage 5'h0A PMBus address (ADDR voltage) 5'h0B VFB of Rail B 5'h0C VDIFF of Rail B 5'h0D IMONB voltage 5'h0E PSYS voltage 5'h0F VFB of Rail C 5'h10 VDIFF of Rail C 5'h11 IMONC voltage 5'h12 Temp voltage 5'h13 Bias on time of Rail A 5'h14 Present VID of Rail A 5'h15 VID + offset in SVID of Rail A 5'h16 Vo_comp of Rail A 5'h17 Bias on time of Rail B 5'h18 Present VID of Rail B 5'h19 VID + offset in SVID of Rail B 5'h1A Vo_comp of Rail B 5'h1B Bias on time of Rail C 5'h1C Present VID of Rail C 5'h1D VID + offset in SVID of Rail C 5'h1E Vo_comp of Rail C For example, to read V_{IN} , write 2Ch to 16'h 3000, and then read 2Ch to get {5'h06 , temp_cmp_sync10mhz , V_{IN} }.

MFR_ADC_SET (2Dh)

The MFR_ADC_SET command on Page 0 is used to configure the ADC result trim and hold time. The TRIM_AD_RESULT command on Page 0 is added to the ADC result directly.

Command	MFR_ADC_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	TRIM_AD_RESULT					X	MFR_ADC_HOLD_TIME				

Bits	Bit Name	Description
[15:11]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[10:6]	TRIM_AD_RESULT	Directly added to the ADC result. 1.56mV/LSB. Range from -25mV ~ 23.5mV.
[5]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[4:0]	MFR_ADC_HOLD_TIME	Used to set the time after the last ADC sample (VDIFF, VFB, ...) finishes and waits for at least [4:0]*100ns before the next sample.

MFR_PROTECT_CFG (2Eh)

The MFR_PROTECT_CFG command on Page 0 is used to enable or disable some protection for all rails.

Command	MFR_PROTECT_CFG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X														

Bits	Bit Name	Description
[15:13]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[12]	ss_oc_en	Enable bit of the per-phase current limit during soft start. 1'b0: disable 1'b1: enable
[11]	temp_flt_en	Enable bit of the temp fault protection (Intelli-Phase OC fault) from the analog. 1'b0: disable 1'b1: enable
[10:9]	ovp1_mode_RailC	OVP1 mode selection bit of Rail C. 2'b00 or 10: no action 2'b01: hiccup 2'b11: latch
[8:7]	ovp1_mode_RailB	OVP1 mode selection bit of Rail B. 2'b00 or 10: no action 2'b01: hiccup 2'b11: latch
[6:5]	ovp1_mode_RailA	OVP1 mode selection bit of Rail A. 2'b00 or 10: no action 2'b01: hiccup 2'b11: latch
[4]	ot_flag_en;	Enable bit of the over-temperature protection (OTP). 1'b0: disable 1'b1: enable
[3]	vin_flag_en	Enable bit of V _{IN} OVP and UVP. 1'b0: disable 1'b1: enable
[2]	otp_latch	OTP mode selection bit. 1'b0: hiccup 1'b1: latch
[1]	vin_uvlo_latch	V _{IN} UVP mode selection bit. 1'b0: hiccup 1'b1: latch
[0]	vin_ovp_latch	V _{IN} OVP mode selection bit. 1'b0: hiccup 1'b1: latch

MFR_DEBUG (2Fh)

The MFR_DEBUG command on Page 0 is used to debug the chip.

Command	MFR_DEBUG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r	r/w	r	r/w	r/w	r/w	r/w	r/w	r/w
Function								X		X		MFR_TRI_STATE_DELAY				

Bits	Bit Name	Description
[15:14]	MFR_EN_0DH	Enable bit for SVID to read 1Bh in 0Dh domain. 2'b00 or 01: disable 0Dh 2'b10: enable 0Dh if Rail A ~ Rail C has 00h address 2'b11: enable 0Dh without 00h address
[13]	Ignore_tempcmp_startup	Enable bit to ignore waiting for the analog temp pin to be ready at start-up. Only includes digital temp comparing. 1'b0: includes analog temp pin comparing 1'b1: does not include analog temp pin comparing
[12]	ignore_prot_restart	Enable bit to ignore V_{IN} and temperature protections. Does not need to wait for V_{IN} and the temp to be ready during restart. 1'b0: disable 1'b1: enable
[11]	ignore_prot_startup	Enable bit to ignore V_{IN} and temperature protection. Does not need to wait for V_{IN} and temp to be ready during start-up. 1'b0: disable 1'b1: enable
[10]	div2_en	Selects VDIFF to be above or below VREF 30mV or 15mV to trigger p30/n30. 1'b0: 30mV 1'b1: 15mV
[9]	MFR_STORE_SVID_CMD_EN	Enable bit to store SVID command (not Get80h/81h/82h) to SVID addresses of 80h/81h/82h. 1'b0: disable 1'b1: enable
[8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7]	bg_chop_en	Enable bit of the bandgap chop. 1'b0: disable 1'b1: enable
[6]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[5]	MFR_SDM_FRAC_EN/ DBG_PWM	Enable bit of DLL, which can make the on time 1.25ns per step. 1'b0: disable 1'b1: enable
[4:0]	MFR_TRI_STATE_DELAY	Sets the delay time for PWM to enter tri-state from a low level. 10ns/LSB.

VIN_ON (35h)

The VIN_ON command on Page 0 is used to set the V_{IN} UVLO rising threshold.

Command	VIN_ON															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED					X	X	X	VIN_ON							

Bits	Bit Name	Description
[15:11]	FIXED	Read only, fixed at -3 (dec) = 11101 (bin).
[10:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VIN_ON	Used to set the V_{IN} on level when V_{IN} is rising. 0.125V/LSB. For example, to set V_{IN} on at 5V, write 35h to E828h.

VIN_OFF (36h)

The VIN_OFF command on Page 0 is used to set the V_{IN} UVLO falling threshold.

Command	VIN_OFF															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED					X	X	X	VIN_OFF							

Bits	Bit Name	Description
[15:11]	FIXED	Read only, fixed at -3 (dec) = 11101 (bin).
[10:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VIN_OFF	Sets the V _{IN} off level when V _{IN} is falling. 0.125V/LSB. For example, to set V _{IN} off at 4V, write 35h to E820h.

IOUT_CAL_GAIN (38h)

The IOUT_CAL_GAIN command on Page 0 is used to set the Rail A PMBus I_{OUT} report gain and can be calculated with Equation (10):

$$IOUT_CAL_GAIN = \frac{K_{CS} * R_{imon} * 2^{15}}{32 * 1000 * k} \quad (10)$$

Where K_{CS} is the CS gain of the Intelli-Phase (in μA/A) (e.g.: MP86901C K_{CS} = 10μA/A), R_{imon} is the resistor connected to IMON (in kΩ), and k is a coefficient according to ICCMAX.

Command	IOUT_CAL_GAIN															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	k					IOUT_CAL_GAIN										

Bits	Bit Name	Description
[15:11]	k	k = 1, IOUT_CAL_GAIN[15:11] = 5'b10001, when 20A ≤ ICCMAX, k = 2, IOUT_CAL_GAIN[15:11] = 5'b10010, when 10A ≤ ICCMAX < 20A k = 4, IOUT_CAL_GAIN[15:11] = 5'b10011, when 5A ≤ ICCMAX < 10A
[10:0]	IOUT_CAL_GAIN	Sets the Rail A PMBus I _{OUT} report gain.

IOUT_CAL_OFFSET (39h)

The IOUT_CAL_OFFSET command on Page 0 is used to set the Rail A PMBus I_{OUT} report offset.

Command	IOUT_CAL_OFFSET															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED					X	X	X	X	X	IOUT_CAL_OFFSET					

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to -1 (dec) = 11111 (bin).
[10:6]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[5:0]	IOUT_CAL_OFFSET	Signed value to set the PMBus I _{OUT} report offset. 0.5A/LSB. Default value is 0. Bit[5] is the sign bit. For example, write 1111100000111110b = F83Eh to 39h to add -1A offset on the PMBus I _{OUT} report.

VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command on Page 0 is used to set the V_{IN} OVP threshold. Once the sensed input voltage exceeds the limit, the system takes action according to the V_{IN} OVP mode.

Command	VIN_OV_FAULT_LIMIT (0.125V/LSB)															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED					X	X	X	VIN_OV_FAULT_LIMIT							

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to -3 (dec) = 11101 (bin).
[10:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VIN_OV_FAULT_LIMIT	Sets the V _{IN} OVP level. 0.125V/LSB. For example, to set V _{IN} on at 24V, write 55h to 1110100011000000b = E8C0h.

VIN_UV_WARNING_LIMIT (58h)

The VIN_UV_WARNING_LIMIT command on Page 0 is used to set the V_{IN} UV warning threshold. Once the sensed input voltage is under the limit, the system indicates that V_{IN} is too low.

Command	VIN_UV_WARN_LIMIT (0.125V/LSB)															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED					X	X	X	VIN_UV_WARNING_LIMIT							

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to -3 (dec) = 11101 (bin).
[10:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VIN_UV_WARNING_LIMIT	Sets the V _{IN} UV warning level. 0.125V/LSB. For example, to set V _{IN} on at 4.5V, write 55h to 1110100000100100b = E824h.

SVID_REG_80H_81H (72h)

The SVID_REG_80H_81H command on Page 0 stores part of the SVID command (not including GetReg 80h/81h/82h), which is stored in the SVID addresses of 80h and 81h.

Command	SVID_REG_80H_81H															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	SVID_REG_80H					SVID_REG_81H						

Bits	Bit Name	Description
[15:12]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[11:8]	SVID_REG_80H	Stores the address of the received SVID command.
[7:0]	SVID_REG_81H	Bit[7] is used to store the frame error flag. Bit[6] is used to store the parity error flag. Bit[5] is used to store the parity in the command. Bit[4:0] is used to store the 5-bit CMD in the SVID command.

SVID_REG_82H (73h)

The SVID_REG_82H command on Page 0 stores part of the SVID command (not including GetReg 80h/81h/82h), which is stored in the SVID addresses of 82h.

Command	SVID_REG_82H							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	SVID_REG_82H							

Bits	Bit Name	Description
[7:0]	SVID_REG_82H	Stores the received SVID command payload.

SLAVE_ADDR (74h)

The WRFAIL command on Page 0 is the latched WRFAIL signal from the MTP, which can only be reset by writing the MTP. The SLAVE_ADDR command on Page 0 is the final address of the PMBus.

Command	SLAVE_ADDR							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	WRFAIL	SLAVE_ADDR						

Bits	Bit Name	Description
[7]	WRFAIL	Flag that indicates the internal write operation is out of time or not when written to MTP.
[6:0]	SLAVE_ADDR	Final slave address of the PMBus.

MFR_CS_1_2 (75h)

The MFR_CS_1_2 command on Page 0 is for phase 1/2 current monitoring via the PMBus.

Command	MFR_CS_1_2															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	MFR_CS_1								MFR_CS_2							

Bits	Bit Name	Description
[15:8]	MFR_CS_1	Shows the monitored current connected to CS1. 0.5A/LSB.
[7:0]	MFR_CS_2	Shows the monitored current connected to CS2. 0.5A/LSB.

MFR_CS_3_4 (76h)

The MFR_CS_3_4 command on Page 0 is for phase 3/4 current monitoring via the PMBus.

Command	MFR_CS_3_4															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	MFR_CS_3								MFR_CS_4							

Bits	Bit Name	Description
[15:8]	MFR_CS_3	Shows the monitored current connected to CS3. 0.5A/LSB.
[7:0]	MFR_CS_4	Shows the monitored current connected to CS4. 0.5A/LSB.

MFR_CS_5_6 (77h)

The MFR_CS_5_6 command Page 0 is for phase 5/6 current monitoring via the PMBus.

Command	MFR_CS_5_6															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	MFR_CS_5								MFR_CS_6							

Bits	Bit Name	Description
[15:8]	MFR_CS_5	Shows the monitored current connected to CS5. 0.5A/LSB.
[7:0]	MFR_CS_6	Shows the monitored current connected to CS6. 0.5A/LSB.

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 0 is a combined register of the output voltage fault flags for Rail A.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x	x			x	x	x
Default	0	x	x	0	0	x	x	x

Bits	Bit Name	Description
[7]		OVP flag. This bit is 1 if OVP is tripped.
[6]		Reserved.
[5]		Reserved.
[4]		UVP flag. This bit is 1 if UVP is tripped.
[3]		Vout_max_warning. The value is written into PMBus 21h 25h/26h, which is larger than MFR_VOUT_MAX.
[2:0]		Reserved.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 0 is a combined register of the output current fault flags for Rail A.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x		x	x	x	x	x
Default	0	x	0	x	x	x	x	x

Bits	Bit Name	Description
[7]		OCP flag. This bit is 1 if OCP is tripped.
[6]		Reserved.
[5]		Phase current limit flag. This bit is 1 if the per-phase current limit is reached.
[4:0]		Reserved.

STATUS_INPUT (7Ch)

The STATUS_INPUT command on Page 0 is a combined register of the input voltage fault flags for the complete regulator.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x	x		x	x	x	x
Default	0	x	x	0	x	x	x	x

Bits	Bit Name	Description
[7]		V _{IN} OVP flag. This bit is 1 if V _{IN} OVP is tripped.
[6]		Reserved.
[5]		V _{IN} UVLO flag. This bit is 1 if V _{IN} UVLO is tripped.
[4:0]		Reserved.

READ_VIN (88h)

The READ_VIN command on Page 0 is used to monitor the input voltage.

Command	READ_VIN (0.125V/LSB)															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	FIXED						X	X	X	READ_VIN						

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to 11101 (bin) = -3 (dec).
[10:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	READ_VIN	Monitors the input voltage. 0.125V/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on Page 0 is used to return the sensed VDIFF voltage of Rail A in VID format.

Command	READ_VOUT															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	X	READ_VOUT							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	READ_VOUT	Shows the sensed VDIFF voltage of Rail A in VID format.

READ_IOUT (8Ch)

The READ_IOUT command on Page 0 reflects the PMBus monitor Rail A total average output current.

Command	READ_IOUT (0.25A/LSB)															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	FIXED					READ_IOUT										
Bits	Bit Name					Description										
[15:11]	FIXED					Fixed to 11110 (bin) = -2 (dec).										
[10:0]	READ_IOUT					Shows the total average output current of Rail A monitored by the PMBus. 0.25A/LSB.										

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command on Page 0 is used to monitor the power stage temperature. The MP2949A monitors the power stage temperature by sensing the voltage on TEMP.

Command	READ_TEMPERATURE															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	X	READ_TEMPERATURE							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	READ_TEMPERATURE	Shows the sensed temperature from TEMP. 1°C/LSB.

READ_POUT (96h)

The READ_POUT command on Page 0 is used to monitor the Rail A output power.

Command	READ_POUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	READ_POUT								

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	READ_POUT	Shows the monitored output power of Rail A by the PMBus. 0.5W/LSB.

READ_PIN (97h)

The READ_PIN command on Page 0 is used to monitor the system total input power. The MP2949A monitors the input power by sensing the voltage on PSYS.

Command	READ_PIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	READ_PIN								

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	READ_PIN	Shows the monitored system total input power. 0.5W/LSB.

MFR_VIN_HYS (B8h)

The MFR_VIN_HYS command on Page 0 is used to set the V_{IN} sense hysteresis and V_{IN} sense offset. The V_{IN} sample result is equal to the ADC result plus the MFR_VIN_SENSE_OFFSET. MFR_VIN_HYS is the threshold for input voltage sample result variation to trigger on-time calculation.

Command	MFR_VIN_HYS							
Format	HYS: unsigned binary; OFFSET: signed binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_VIN_HYS				MFR_VIN_SENSE_OFFSET			

Bits	Bit Name	Description
[7:4]	MFR_VIN_HYS	Sets the threshold for V_{IN} sample result variation to trigger on-time calculation. The on time is refreshed when the V_{IN} sample variation is larger than MFR_VIN_HYS. 6.25mV/LSB.
[3:0]	MFR_VIN_SENSE_OFFSET	Sets the V_{IN} sample offset. Bit[3] is the sign bit. 25mV/LSB.

MFR_1PHL (BBh)

The MFR_1PHL command on Page 0 is used to set the phase shedding level of the total current. MFR_1PHL is 1-phase CCM's level. 2- to 6-phase CCM's level is MFR_1PHL * phase number. 1-phase DCM's level is fixed at 5A.

Command	MFR_1PHL							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	MFR_1PHL				

Bits	Bit Name	Description
[7:5]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[4:0]	MFR_1PHL	Sets the phase shedding level of 1-phase CCM. 1A/LSB.

MFR_PHASE_HYS (BCh)

The MFR_PHASE_HYS command on Page 0 is used to set the hysteresis value during phase adding.

Command	MFR_PHASE_HYS							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_PHASE_HYS			

Bits	Bit Name	Description
[7:4]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[3:0]	MFR_PHASE_HYS	It is used to set the hysteresis value during phase adding. 1A/LSB.

For example, if MFR_1PHL (BBh) = 11h (17A) and MFR_PHASE_HYS (BCh) = 05h (5A), then the phase shedding threshold is 51A and the phase adding threshold is 56A from 4-phase to 3-phase (see Figure 19).

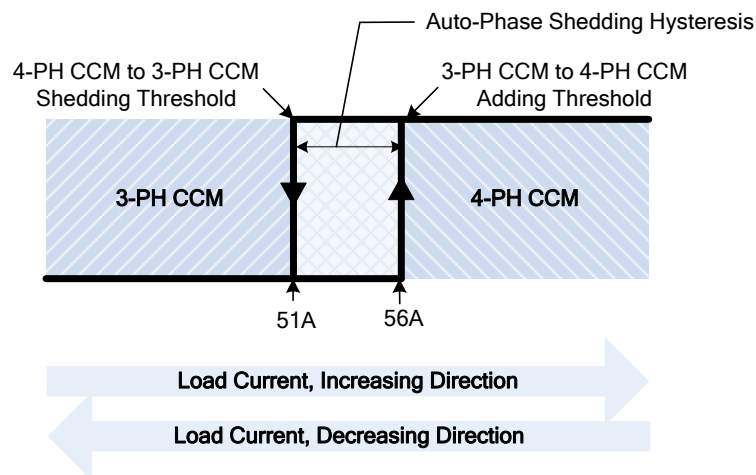


Figure 19: Phase Shedding and Adding Operation

PROTOCOL_ID_RD_RC_TA, ENABLE_TO_SVID_RDY_VR (BDh)

PROTOCOL_ID_RD_RC_TA[15:8] is used to set the lower four bits of PROTOCOL_ID of the PSYS domain (Rail D) and Rail C. The ENABLE_TO_SVID_RDY_VR command on Page 0 is used to set the time length from EN's positive edge to the time VR is ready to receive the SVID command according to the Intel spec. Its format is the same as the SVID spec.

Command	PROTOCOL_ID_RD_RC_TA															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PROTOCOL_ID RD				PROTOCOL_ID RC				ENABLE_TO_SVID_RDY_VR							

Bits	Bit Name	Description
[15:12]	PROTOCOL_ID RD	Provides Rail D's lower four bits of PROTOCOL_ID, which show what version of the SVID protocol Rail D can support.
[11:8]	PROTOCOL_ID RC	Provides Rail C's lower four bits of PROTOCOL_ID, which show what version of the SVID protocol Rail C can support.
[7:0]	ENABLE_TO_SVID_RDY_VR	Sets the time length (in μ s) from EN's positive edge to the time when VR is ready to receive the SVID command. The time length is equal to $[3:0] / 16 * 2^{[7:4]}$.

PS3_PS4_EXIT_DELAY (BEh)

The PS3_PS4_EXIT_DELAY command on Page 0 is used to set the time length of the VR to exit PS3/4. The format is the same as the SVID spec.

Command	PS3_PS4_EXIT_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PS3_EXIT_LATENCY_VR								PS4_EXIT_LATENCY_VR							

Bits	Bit Name	Description
[15:8]	PS3_EXIT_LATENCY_VR	Sets the time length (in μ s) for Rail A to exit PS3. The time length is equal to $[11:8] / 16 * 2^{[15:12]}$.
[7:0]	PS4_EXIT_LATENCY_VR	Sets the time length (in μ s) that VR takes to exit PS4. The time length is equal to $[3:0] / 16 * 2^{[7:4]}$.

VENDOR_ID_PRODUCT_ID (BFh)

The VENDOR_ID_VR command on Page 0 provides the unique identification for the VR vendor. The vendor ID is assigned by Intel. This register is mandatory, and the VR must return the assigned vendor ID. The PRODUCT_ID_VR command on Page 0 provides the unique identification for the VR product. The VR vendor assigns this number.

Command	VENDOR_ID_PRODUCT_ID															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VENDOR_ID_VR								PRODUCT_ID_VR							

Bits	Bit Name	Description
[15:8]	VENDOR_ID_VR	Provides the unique identification assigned by Intel for the VR vendor.
[7:0]	PRODUCT_ID_VR	Provides the unique identification assigned by the VR vendor for the VR product.

PRODUCT_DATA_CODE (C0h)

The PRODUCT_DATA_CODE command on Page 0 provides the unique four-digit hex code identifier for different customers or different projects of the VR controller. The vendor assigns this data.

Command	PRODUCT_DATA_CODE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PRODUCT_DATA_CODE															

Bits	Bit Name	Description
[15:0]	PRODUCT_DATA_CODE	Provides the unique four-digit hex code identifier assigned by the vendor for different customers and different projects.

CODE_REV_PROTOCOL_RB_RA (C1h)

The CODE_REV command on Page 0 identifies the code revision. PROTOCOL_ID_RB/A are the lower four bits of PROTOCOL_ID of Rail B and Rail A, respectively. These commands identify what version of the SVID protocol the controller supports.

Command	CODE_REV_PROTOCOL_RB_RA															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	CODE_REV								PROTOCOL_ID RB				PROTOCOL_ID RA			

Bits	Bit Name	Description
[15:8]	CODE_REV	Provides the digital code revision assigned by the VR vendor.
[7:4]	PROTOCOL_ID RB	Provides Rail B with the lower four bits of PROTOCOL_ID, which show what version of the SVID protocol Rail B can support.
[3:0]	PROTOCOL_ID RA	Provides Rail A with the lower four bits of PROTOCOL_ID, which show what version of the SVID protocol Rail A can support.

DECAY_CFG_34H_06H (C2h)

The DECAY_CFG is used to set the three rails' decay slew rate. The MUTI_VR_CONFIG command is the initial value of the SVID 34h register. The CAPABILITY_VR command on Page 0 is the bit mapped register, which identifies SVID VR capabilities. The optional telemetry registers are supported.

Command	DECAY_CFG_34H_06H															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X		DECAY_CFG			MUTI_VR_CONFIG		CAPABILITY_VR						

Bits	Bit Name	Description
[15:13]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[12]	STORE MTP FSM	Enable bit to store the mtp_wr state to the SVID registers for debugging. 1b'0: disable 1b'1: enable
[11:10]	DECAY_CFG	Configures the decay slew rate. 2b'00 or 2b'11: normal decay, Hi-Z PWM, or output discharge slew rate depending on output caps and output current. 2b'01: decay with fast slew rate, VREF discharge with fast slew rate when the decay command is received. 2b'10: decay with slow slew rate, VREF discharge with slow slew rate when the decay command is received.
[9:8]	MUTI_VR_CONFIG	Initial value of the lower two bits of SVID MUTI_VR_CONFIG (34h).
[7:0]	CAPABILITY_VR	Shows which of the telemetry registers are supported. A 1 in any bit indicates that an optional function is supported by the slave. Bit[7]: IOUT/JOUT format (15h) Bit[6]: temperature (17h) Bit[5]: input P (1Bh) Bit[4]: input V (1Ah) Bit[3]: input I (19h) Bit[2]: POUT (18h) Bit[1]: VOUT (16h) Bit[0]: IOUT (15h)

TOLERANCE_SR_FAST (C3h)

The MFR_VR_TOLERANCE command on Page 0 is used to set the Rail A output tolerance (binary format in mV). The SR_FAST_VR command on Page 0 is used to set the data register containing the Rail A fast slew rate capability of the slew rate the platform VR can sustain (binary format in mV/μs).

Command	TOLERANCE_SR_FAST															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_VR_TOLERANCE								SR_FAST_VR							

Bits	Bit Name	Description
[15:8]	MFR_VR_TOLERANCE	Shows the Rail A output tolerance. 1mV/LSB.
[7:0]	SR_FAST_VR	Shows the fast slew rate that Rail A supports. 1mV/μs per LSB.

MFR_VOUT_MAX_9BIT (C4h)

The MFR_VOUT_MAX_9BIT command on Page 0 is used to set the Rail A upper limit of VID + OFFSET. In PMBus mode, if VID + OFFSET is higher than this limit, the command is acknowledged, the output is clamped at this limit. In SVID mode, if VID + OFFSET is higher than this limit, this command is rejected, and the output holds the voltage before the command.

Command	MFR_VOUT_MAX_9BIT															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	MFR_VOUT_MAX_9BIT								

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	MFR_VOUT_MAX_9BIT	Sets the Rail A upper limit of VID + OFFSET.

IVID2_1_I_DEF (C5h)

The iver2_i_def command on Page 0 is the default value of the Rail A maximum current (1A/bit) expected when VID is set as IVID2 - VID ≥ VID > IVID3 - VID. The iver1_i_def command on Page 0 is the Rail A default value of the maximum current (1A/bit) expected when VID is set as IVID1 - VID ≥ VID > IVID2 - VID.

Command	IVID2_1_I_DEF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	iver2_i_def								iver1_i_def							

Bits	Bit Name	Description
[15:8]	iver2_i_def	Sets the Rail A default value of the maximum current expected when VID is set as IVID2 - VID ≥ VID > IVID3 - VID. 1A/LSB.
[7:0]	iver1_i_def	Sets the Rail A default value of the maximum current expected when VID is set as IVID1 - VID ≥ VID > IVID2 - VID. 1A/LSB.

PIN_MAX_IVID3_I_DEF (C6h)

The MFR_PIN_MAX command on Page 0 is the input power sensor scaling for the SVID 1Bh (PSYS) register, programmed by the platform designer to the rating of the input power sensor (1W/LSB). The SVID PIN_MAX register (2Eh) is half of MFR_PIN_MAX. ival3_i_def is the default value of the Rail A maximum current (1A/bit) expected when VID is set as IVID3 - VID ≥ VID.

Command	PIN_MAX_IVID3_I_DEF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_PIN_MAX								Ivid3_i_def (1A/LSB)							

Bits	Bit Name	Description
[15:8]	MFR_PIN_MAX	Sets the system input power sensor scaling. 1W/LSB.
[7:0]	ival3_i_def	Sets the Rail A default value of the maximum current expected when VID is set as IVID3 - VID ≥ VID. 1A/LSB.

MFR_PHASE_CFG (CAh)

The MFR_PHASE_CFG (CAh) command on Page 0 is used to set the phase configuration of the VR. The PWM can be active only when both the rail and MFR_PHASE_CFG are enabled. The PWM distribution of Rail A shown below is under CBh[15] = 1.

Command	MFR_PHASE_CFG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	RAILC_EN	RAILB_EN	RAILA_EN	MFR_PHASE_CFG				

Bits	Bit Name	Description
[7]	RAILC_EN	Enable bit of Rail C. 1'b0: disable Rail C 1'b1: enable Rail C
[6]	RAILB_EN	Enable bit of Rail B. 1'b0: disable Rail B 1'b1: enable Rail B
[5]	RAILA_EN	Enable bit of Rail A. 1'b0: disable Rail A 1'b1: enable Rail A
[4:0]	MFR_PHASE_CFG	MFR_PHASE_CFG
		PWM Distribution of Rail A
		PWM Distribution of Rail B
		PWM Distribution of Rail C
		5b'00000
		1, 2, 3, 4, 5, 6
		-
		-
		5b'00001
		1, 2, 3, 4, 6
		5
		-
		-
		5b'00010
		1, 2, 3, 4, 6
		-
		-
		5b'00011
		1, 2, 3, 4
		5, 6
		-
		5b'00100
		1, 2, 3, 4
		5
		6
		5b'00101
		1, 2, 3, 4
		5
		-
		5b'00110
		1, 2, 3, 4
		-
		-
		5b'00111
		1, 2, 3
		4, 5
		6
		5b'01000
		1, 2, 3
		4, 5
		-
		5b'01001
		1, 2, 3
		5
		6
		5b'01010
		1, 2, 3
		5
		-
		-
		5b'01011
		1, 2, 3
		-
		-
		5b'01100
		1, 2
		4, 5
		6
		5b'01101
		1, 2
		4, 5
		-
		5b'01110
		1, 2
		5
		6
		5b'01111
		1, 2
		5
		-
		5b'10000
		1, 2
		-
		-
		5b'10001
		1
		5
		6
		5b'10010
		1
		5
		-
		-
		5b'10011
		1
		-
		-
		Others
		-
		-
		-

T_DC_DROPPH_V_LOWFS (CBh)

The MFR_DC_CNT command on Page 0 is used to control the phase dropping time and delay time of turning on the DC calibration function for the three rails. The MFR_VREF_DS_FSLow command is used set the low VID level to disable the hold DC loop.

Command	T_DC_DROPPH_V_LOWFS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_DC_CAL_CNT				DROP_PHASE				MFR_VREF_DS_FSLow							

Bits	Bit Name	Description
[15]	RAILA_PWM_EN	Enable bit of the PWMs (under the configuration of CAh) except PWM1 of Rail A. For example, if CAh is written to E7h, and RAILA_PWM_EN is 0, then only Rail A PWM1 is active, and PWM2 and PWM3 are disabled. However, PWM1, PWM2, and PWM3 are active if RAILA_PWM_EN is 1.
[14:11]	MFR_DC_CNT	Sets the time length to enable the DC loop after the DC loop is disabled caused by any transient, SetVID_Fast/Slow, decay, SetPS, or PWM high/low at CCM. One whole sample period/LSB.
[10:8]	DROP_PHASE	Sets the delay time to the droop phase after the total current is detected to be smaller than the phase shedding threshold. One whole sample period/LSB.
[7:0]	MFR_VREF_DS_FSLow	Sets the VREF level under which the VR disables the function optionally to hold the DC loop if the PWM frequency low is triggered. VID format.

DC_CTRL_ADP_CTRL (CCh)

The command DC_CTRL_ADP_CTRL on Page 0 is used hold the current balance, hold the DC loop, and exit APS when a dynamic case occurs.

Command	DC_CTRL_ADP_CTRL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	MFR_DC_CTRL										DELAY_TIME_SET			

Bits	Bit Name	Description
[15:14]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[13]	MFR_DC_CTRL[3]	Holds the Rail A DC loop for a given time, CBh[14:11], when the frequency is lower than that set by CFh[8:0], and VID is lower than that set by CBh[7:0] under PS0/PS1 (related register in Page 0). 1'b1: hold DC loop if CCh[10] = 1, enable DC loop if CCh[10] = 0 1'b0: enable DC loop if CCh[10] = 1, enable DC loop if CCh[10] = 0
[12]	MFR_DC_CTRL[2]	Enable bit to hold the DC calibration during the load transient. 1'b0: disable 1'b1: enable
[11]	MFR_DC_CTRL[1]	Rail A enable bit to hold the DC calibration during SetVID_Fast/Slow, Set_PS, and decay. 1'b0: disable 1'b1: enable
[10]	MFR_DC_CTRL[0]	Rail A enable bit to hold the DC calibration when the PWM frequency is lower than that set by CFh[8:0] or the PWM frequency is higher than that set by CDh[13:6] during CCM. 1'b0: disable 1'b1: enable
[9]	MFR_ADP_OC_EXIT_EN	Rail A enable bit for 1-phase CCM/DCM to exit and enter full-phase when per-phase over-current occurs on the rail. 1'b0: disable 1'b1: enable
[8]	MFR_ADP_PSI_BYPASS	Disables the Rail A Set_PS command when auto-phase shedding is enabled (not including IVID). 1'b0: enable 1'b1: disable
[7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6]	MFR_DYNAMIC_FLT[6]	Enable bit of Rail A to exit APS and hold the current balance during the load transient. 1'b0: disable 1'b1: enable
[5]	MFR_DYNAMIC_FLT[5]	Enable bit of Rail A to exit APS and hold the current balance when Rail A receives a SetVID_Fast/Slow and decay command. 1'b0: disable 1'b1: enable
[4]	MFR_DYNAMIC_FLT[4]	Enable bit of Rail A to exit APS and hold current balance when the Rail A PWM frequency is lower or higher than the setting threshold. 1'b0: disable 1'b1: enable
[3:0]	DELAY_TIME_SET	Sets the delay time to enable the current balance after the load transient. 20μs/LSB.

HF_PFM_SLP_DISCHG (CDh)

The MFR_HF_CYCLE command on Page 0 is used to set the PWM frequency high level threshold for the three rails. If the PWM period is shorter than the high level, then the switch frequency is high. The DISCHG_TIME and DISCHG_NUM command on Page 0 is used to set the slope ramp discharge time and discharge MOSFET number of Rail A.

Command	HF_PFM_SLP_DISCHG															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	MFR_HF_CYCLE								DISCHG_TIME			DISCHG_NUM		

Bits	Bit Name	Description
[15:14]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[13:6]	MFR_HF_CYCLE	Sets the detected switch high frequency threshold for the three rails.
[5:3]	DISCHG_TIME	Sets the Rail A internal slope ramp discharge time. 10ns/LSB.
[2:0]	DISCHG_NUM	Sets the Rail A internal slope ramp discharge MOSFET number.

MINOFF_BLANK_TIME (CEh)

The MFR_MINON_TIME command on Page 0 is to control the minimum PWM on pulse for the three rails. The MFR_MINOFF_TIME command on Page 0 is to control the minimum interval time between the adjacent PWM on pulse of the same phase for the three rails. The MFR_BLANK_TIME command on Page 0 is used to control the minimum interval time between the adjacent phases in the same rail for the three rails.

Command	MINOFF_BLANK_TIME															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_MINON_TIME			MFR_MINOFF_TIME								MFR_BLANK_TIME				

Bits	Bit Name	Description
[15:13]	MFR_MINON_TIME	Sets the minimum PWM width for three rails. 5ns/LSB.
[12:6]	MFR_MINOFF_TIME	Sets the minimum time between the last PWM falling edge and the next PWM rising edge of the same phase for three rails. 10ns/LSB.
[5:0]	MFR_BLANK_TIME	Sets the minimum time between the adjacent phase PWM of the same rail for the three rails. 10ns/LSB.

MFR_PFM_SET (CFh)

The MFR_LF_CYCLE command on Page 0 defines the low PWM frequency threshold. If the time length between the adjacent PWM of the same phase is longer than that set by MFR_LF_CYCLE, then the switch frequency is low. PFM_LOW/HIGH_EN_Rx on Page 0 controls the low/high switch frequency function for the three rails.

Command	MFR_PFM_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X						MFR_LF_CYCLE									

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14]	PFM_LOW_EN_RC	Enable bit of detecting the switch frequency low of Rail C. 1b'0: disable 1b'1: enable
[13]	PFM_HIGH_EN_RC	Enable bit of detecting the switch frequency high of Rail C. 1b'0: disable 1b'1: enable
[12]	PFM_LOW_EN_RB	Enable bit of detecting the switch frequency low of Rail B. 1b'0: disable 1b'1: enable
[11]	PFM_HIGH_EN_RB	Enable bit of detecting the switch frequency high of Rail B. 1b'0: disable 1b'1: enable
[10]	PFM_LOW_EN_RA	Enable bit of detecting the switch frequency low of Rail A. 1b'0: disable 1b'1: enable
[9]	PFM_HIGH_EN_RA	Enable bit of detecting the switch frequency high of Rail A. 1b'0: disable 1b'1: enable
[8:0]	MFR_LF_CYCLE	Sets the detected switch low frequency threshold. 10ns/LSB.

MFR_SLOPE_SR_6P (D0h)

The MFR_SLOPE_SR_6P command on Page 0 is used to set the slew rate of slope ramp compensation for 6-phase operation.

Command	MFR_SLOPE_SR_6P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_6P				CURRENT_SOURCE_6P				

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:6]	CAP_6P	Sets the cap number for slope voltage generation at 6-phase CCM operation. The capacitance is equal to $(8 - \text{DEC}(\text{CAP_6P})) \times 3.7\text{pF}$.
[5:0]	CURRENT_SOURCE_6P	Sets the current source for the slope voltage generation at 6-phases CCM operation. 0.25μA/LSB (design value, subject to change after bench data collection).

MFR_SLOPE_CNT_6P (D1h)

The MFR_SLOPE_CNT_6P command on Page 0 is used to set the saturate value of slope ramp compensation during 6-phase operation.

Command	MFR_SLOPE_CNT_6P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_6P									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_SLOPE_CNT_6P	Sets the slope compensation saturation time for 6-phase CCM. 10ns/LSB. Generally, this bit is set at $1.3 \times (T_s/6 - T_{blank})$ time, where T_s is the switching period time, and T_{blank} is the PWM blanking time.

MFR_SLOPE_SR_5P (D2h)

The MFR_SLOPE_SR_5P command on Page 0 is used to set the slew rate of slope ramp compensation during 5-phase operation.

Command	MFR_SLOPE_SR_5P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_5P				CURRENT_SOURCE_5P				

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:6]	CAP_5P	Sets the cap number for the slope voltage generation at 5-phase CCM operation. The capacitance is equal to $(8 - \text{DEC}(\text{CAP_5P})) \times 3.7\text{pF}$.
[5:0]	CURRENT_SOURCE_5P	Sets the current source for the slope voltage generation at 5-phase CCM operation. 0.25 μA /LSB (design value, subject to change after bench data collection).

MFR_SLOPE_CNT_5P (D3h)

The MFR_SLOPE_CNT_5P command on Page 0 is used to set the saturate value of slope ramp compensation during 5-phase operation.

Command	MFR_SLOPE_CNT_5P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_5P									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_SLOPE_CNT_5P	Sets the slope compensation saturation time for 5-phase CCM. 10ns/LSB. Generally, it is set at $1.3 \times (T_s/5 - T_{blank})$ time, where T_s the switching period time, and T_{blank} is the PWM blanking time.

MFR_SLOPE_SR_4P (D4h)

The MFR_SLOPE_SR_4P command on Page 0 is used to set the slew rate of slope ramp compensation during 4-phase operation.

Command	MFR_SLOPE_SR_4P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_4P				CURRENT_SOURCE_4P				

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:6]	CAP_4P	Sets the cap number for slope voltage generation at 4-phase CCM operation. The capacitance is equal to $(8 - \text{DEC}(\text{CAP_4P})) \times 3.7\text{pF}$.
[5:0]	CURRENT_SOURCE_4P	Sets the current source for slope voltage generation at 4-phase CCM operation. 0.25 μA /LSB (design value, subject to change after bench data collection).

MFR_SLOPE_CNT_4P (D5h)

The MFR_SLOPE_CNT_4P command on Page 0 is used to set the saturate value of slope ramp compensation during 4-phase operation.

Command	MFR_SLOPE_CNT_4P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_4P									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_SLOPE_CNT_4P	Sets the slope compensation saturation time for 4-phase CCM, 10ns/LSB. Generally, this bit is set at $1.3 \times (T_s/4 - T_{\text{blank}})$ time, where T_s the switching period time, and T_{blank} is the PWM blanking time.

MFR_SLOPE_SR_3P (D6h)

The MFR_SLOPE_SR_3P command on Page 0 is used to set the slew rate of slope ramp compensation during 3-phase operation.

Command	MFR_SLOPE_SR_3P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_3P				CURRENT_SOURCE_3P				

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:6]	CAP_3P	Sets the cap number for slope voltage generation at 3-phase CCM operation. The capacitance is equal to $(8 - \text{DEC}(\text{CAP_3P})) \times 3.7\text{pF}$.
[5:0]	CURRENT_SOURCE_3P	Sets the current source for slope voltage generation at 3-phase CCM operation. 0.25 μA /LSB (design value, subject to change after bench data collection).

MFR_SLOPE_CNT_3P (D7h)

The MFR_SLOPE_CNT_3P command on Page 0 is used to set the saturate value of slope ramp compensation during 3-phase operation.

Command	MFR_SLOPE_CNT_3P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_3P									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_SLOPE_CNT_3P	Sets the slope compensation saturation time for 3-phase CCM. 10ns/LSB. Generally, this time is set at $1.3 \times (T_s/3 - T_{blank})$ time, where T_s the switching period time, and T_{blank} is the PWM blanking time.

MFR_SLOPE_SR_2P (D8h)

The MFR_SLOPE_SR_2P command on Page 0 is used to set the slew rate of slope ramp compensation during 2-phase operation.

Command	MFR_SLOPE_SR_2P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_2P				CURRENT_SOURCE_2P				
Bits	Bit Name				Description											
[15:9]	RESERVED				Unused. X indicates writes are ignored and always read as 0.											
[8:6]	CAP_2P				It is used to set the cap number for slope voltage generation at 2-phase CCM operation. The capacitance is equal to (8 - DEC (CAP_2P)) x 3.7pF.											
[5:0]	CURRENT_SOURCE_2P				It is used to set the current source for slope voltage generation at 2-phase CCM operation. 0.25μA/LSB (design value, subject to change after bench data collection).											

MFR_SLOPE_CNT_2P (D9h)

The MFR_SLOPE_CNT_2P command on Page 0 is used to set the saturate value of the slope ramp compensation during 2-phase operation.

Command	MFR_SLOPE_CNT_2P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_2P									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_SLOPE_CNT_2P	Sets the slope compensation saturation time for 2-phase CCM. 10ns/LSB. Generally, this time is set at 1.3 x (Ts/2-Tblank) time, where Ts the switching period time, and Tblank is the PWM blanking time.

Figure 20 shows a slope voltage curve at 2-phase CCM.

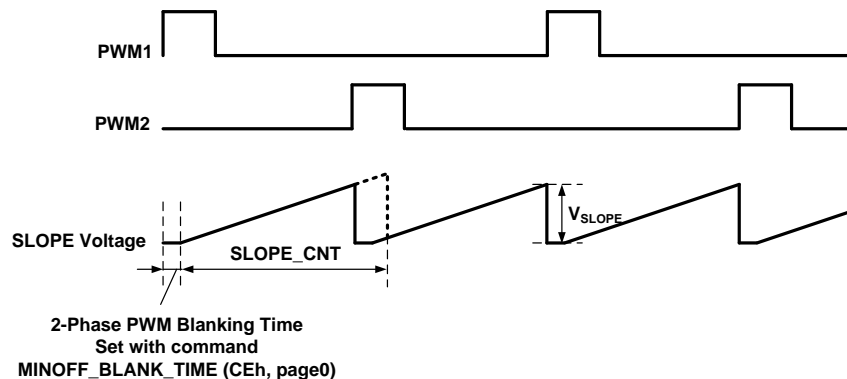


Figure 20: Slope Voltage at 2-Phase CCM Power State

MFR_SLOPE_SR_1P (DAh)

The MFR_SLOPE_SR_1P command on Page 0 is used to set the slew rate of slope ramp compensation during 1-phase operation.

Command	MFR_SLOPE_SR_1P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_1P			CURRENT_SOURCE_1P					

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:6]	CAP_1P	Sets the cap number for slope voltage generation at 1-phase CCM operation. The capacitance is equal to (8 - DEC (CAP_1P)) x 3.7pF.
[5:0]	CURRENT_SOURCE_1P	Sets the current source for slope voltage generation at 1-phase CCM operation. 0.25μA/LSB (design value, subject to change after bench data collection).

MFR_SLOPE_CNT_1P (DBh)

The MFR_SLOPE_CNT_1P command on Page 0 is used to set the saturate value of slope ramp compensation during 1-phase operation.

Command	MFR_SLOPE_CNT_1P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_1P									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_SLOPE_CNT_1P	Sets the slope compensation saturation time for 1-phase CCM. 10ns/LSB. Generally, this time is set at 1.3 x (Ts - Tblank) time, where Ts the switching period time, and Tblank is the PWM blanking time.

MFR_SLOPE_SR_DCM (DCh)

The MFR_SLOPE_SR_DCM command on Page 0 is used to set the slew rate of slope ramp compensation during 1-phase DCM operation.

Command	MFR_SLOPE_SR_DCM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_DCM			CURRENT_SOURCE_DCM					

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:6]	CAP_DCM	Sets the cap number for slope voltage generation at 1-phase DCM operation. The capacitance is equal to (8 - DEC (CAP_DCM)) x 3.7pF.
[5:0]	CURRENT_SOURCE_DCM	Sets the current source for slope voltage generation at 1-phase DCM operation. 0.25μA/LSB (design value, subject to change after bench data collection).

MFR_SLOPE_CNT_DCM (DDh)

The MFR_SLOPE_CNT_DCM command on Page 0 is used to set the saturate value of slope compensation during 1-phase DCM operation.

Command	MFR_SLOPE_CNT_DCM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_DCM									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_SLOPE_CNT_DCM	Sets the slope compensation saturation time for 1-phase DCM. 10ns/LSB. Generally, this time is set at 2 x (Ts - Tblank) time, where Ts the switching period time, and Tblank is the PWM blanking time.

MFR_TRIM_2_1_DCM (DEh)

The MFR_TRIM_2_1_DCM command on Page 0 is used to trim the Rail A output voltage during 1-phase ~ 2-phase CCM and 1-phase DCM.

Command	MFR_TRIM_2_1_DCM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_TRIM_2					MFR_TRIM_1					MFR_TRIM_DCM				

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:10]	MFR_TRIM_2	Sets the Rail A V _{OUT} trim for 2-phase CCM operation. 2.73mV/LSB.
[9:5]	MFR_TRIM_1	Sets the Rail A V _{OUT} trim for 1-phase CCM operation. 2.73mV/LSB.
[4:0]	MFR_TRIM_DCM	Sets the Rail A V _{OUT} trim for 1-phase DCM operation. 2.73mV/LSB.

MFR_TRIM_5_4_3 (DFh)

The MFR_TRIM_5_4_3 command on Page 0 is used to trim the Rail A output voltage during 3-phase ~ 5-phase CCM.

Command	MFR_PSI_TRIM_5_4_3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_TRIM_5					MFR_TRIM_4					MFR_TRIM_3				

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:10]	MFR_TRIM_5	Sets the V _{OUT} trim for 5-phase CCM operation. 2.73mV/LSB.
[9:5]	MFR_TRIM_4	Sets the V _{OUT} trim for 4-phase CCM operation. 2.73mV/LSB.
[4:0]	MFR_TRIM_3	Sets the V _{OUT} trim for 3-phase CCM operation. 2.73mV/LSB.

MFR_TRIM_6 (E0h)

The MFR_TRIM_6 command on Page 0 is used to trim the Rail A output voltage during 6-phase CCM (2.73mV/LSB).

Command	MFR_PSI_TRIM_6PHASE							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	MFR_TRIM_6				

Bits	Bit Name	Description
[7:5]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[4:0]	MFR_TRIM_6	Sets the V _{OUT} trim for 6-phase CCM operation. 2.73mV/LSB.

SHUTLEVEL_ADDRPMBUS (E1h)

SHUTLEVEL_ADDRPMBUS is the shut level set by MFR_SHUTDOWN_LEVEL, where VREF is lower than the moment V_{OUT} (VREF) is slewing downward. The VR stops switching and starts to decay for the three rails. The MFR_ADDR_PMBUS command on Page 0 is used to configure the PMBus address of device.

Command	SHUTLEVEL_ADDRPMBUS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_SHUTDOWN_LEVEL						X		ADDRPMBUS						

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:9]	MFR_SHUTDOWN_LEVEL	5mV/LSB (5mV mode), 10mV/LSB (10mV mode). For example, to set the shutdown level at 0.16V, set this bit as 6'h20h (5mV/LSB) or 6'h10 (10mV/LSB).
[8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7]	4_LOW_ADDR_REG	Selection bit to choose the four lower bits of the PMBus address set by the register or pin. 1'b0: set PMBus address bit[3] ~ [0] from the pin 1'b1: set PMBus address bit[3] ~ [0] from the register
[6:0]	MFR_ADDR_PMBUS	Sets the four lower bits of the PMBus address.

MFR_CB_SATU_PI (E2h)

The TUNE_NSATU_PSATU command on Page 0 is used to define the negative and positive saturation level of current balance calculation of Rail A. The MFR_CB_PI command is used to set the proportion integrate (PI) value for the current balance.

Command	MFR_CB_SATU_PI															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TUNE_NSATU				TUNE_PSATU				MFR_CB_PI							

Bits	Bit Name	Description
[15:12]	TUNE_NSATU	Defines the negative saturation level of the current balance calculation. 10ns/LSB, range from -80ns ~ 0ns. bit[15] is the sign bit. For example, to set the negative saturation level as -50ns, set E2h [15:12] = 4'hB.
[11:8]	TUNE_PSATU	Defines the positive saturation level of the current balance calculation. 10ns/LSB, range from 0ns ~ 70ns. For example, to set the negative saturation level as 50ns, set E2h [11:8] = 4'h5.
[7:0]	MFR_CB_PI	Sets the Rail A PI parameter value for the current balance.

VTRIM_STEP_VCAL_PI (E3h)

The 5mV_VO_COMP_DECAY command on Page 0 is to configure V_{OUT} compensation (COMP) after DVID for the VR. The MFR_VCAL_PI command is used to set the Rail A PI value for DC calibration.

Command	VTRIM_STEP_VCAL_PI															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																MFR_VCAL_PI

Bits	Bit Name	Description
[15:14]	5mV_VO_COMP_SETP	Sets the V_{OUT} compensation (COMP) adding step by counting the PWM number during SetVID_Fast/Slow. This bit updates every ([15:14] + 1) PWM (PWM1/5/6 for each rail).
[13]	5mV_VO_COMP_SETP_EN	Enable bit to count PWM1/5/6 when adding V_{OUT} compensation, effective when [12] = 1. 1b'0: disable 1b'1: enable
[12]	5mV_VO_COMP_EN	Enable bit to add 5mV V_{OUT} compensation under 5mV mode for the three rails. 1b'0: disable 1b'1: enable
[11:9]	VO_COMP_SETP_EXIT_DECAY	Sets the three rails' V_{OUT} compensation (COMP) adding step by counting the PWM number after decay. This bit updates every [11:9] PWM (PWM1/5/6 for each rail).
[8]	VO_COMP_SETP_EXIT_DECAY_EN	Enable for the three rails to add V_{OUT} compensation (COMP) by counting the PWM after the decay finishes, or V_{OUT} compensation is added once the decay finishes. 1b'0: V_{OUT} compensation (COMP) added once 1b'1: V_{OUT} compensation (COMP) added by counting PWM
[7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6:0]	MFR_VCAL_PI	Sets the PI parameter for DC loop calibration for Rail A.

MFR_VR_CONFIG (E4h)

The MFR_VR_CONFIG command on Page 0 is used to enable the function of Rail A, such as DC loop calibration, auto-phase shedding, etc.

Command	MFR_VR_CONFIG															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
[15]	MFR_SLOPE_LEAKAGE	Enable bit for the three rails to hold the slope ramp after the slope saturates. 1b'0: disable 1b'1: enable
[14]	MFR_PMBUS_SR_SEL	Selection bit of Rail A for the VID slew rate when the PMBus controls V_{OUT} . 1b'0: V_{OUT} changes with fast slew rate when the PMBus controls V_{OUT} . 1b'1: V_{OUT} changes with slow slew rate when the PMBus controls V_{OUT} .
[13]	MFR_WAIT_SETTLE_SEL	Selection bit of the three rails for the time VRRDY turns slow from high when DVID rises from 0V (not include VBOOT) if SVID 34h write to 00. 1b'0: VRRDY turns high when DVID rises from 0V (not include VBOOT) starts. 1b'1: VRRDY turns high after DVID rises from 0V (not include VBOOT) finishes.
[12]	IMVP9_SEL	Selection bit for the three rails to choose IMVP8 or IMVP9. Only affects the VRRDY assignment. 1b'0: IMVP8 1b'1: IMVP9
[11]	DC_LOOP_DCM_EN	Enable bit for Rail A DC's calibration during PS2. Only active when DC_LOOP_EN is enabled. 1b'0: disable 1b'1: enable when bit[10] = 1
[10]	DC_LOOP_EN	Enable bit for Rail A DC calibration. 1b'0: disable 1b'1: enable DC calibration in CCM. Must enable bit[11] for PS2 DC calibration.
[9]	PMBUS_PS_EN	Enable bit for PMBus to control the power state of Rail A in PMBus mode. 1'b0: disable 1'b1: enable
[8:7]	PMBUS_PS	Sets the Rail A power state when PMBus controls the power state. 2'b00: PS0 2'b01: PS1 2'b10: PS2 2'b11: PS3
[6]	TON_REDUCTION_DCM_EN	Enable bit of Rail A to reduce the PS2 on time to 75% of that in PS0. 1'b0: disable 1'b1: enable
[5]	VID_STEP	Selection bit of the VID step for Rail A. 1'b1: 5mV/LSB 1'b0: 10mV/LSB
[4]	IPHASE_BALNCE_EN	Enable bit of the Rail A current balance. 1'b0: disable 1'b1: enable
[3]	MFR_COPYMTP_ENPIN_RESTART	Enable bit for the VR controller to copy MTP after EN restarts with PE = 1. 1'b0: disable 1'b1: enable
[2]	APS_EN	Enable bit of the Rail A auto-phase shedding function. 1'b0: disable 1'b1: enable
[1]	IVID_EN	Enable bit of the Rail A IVID function. 1'b0: disable 1'b1: enable
[0]	PMBUS_MODE_SEL	Selection bit of Rail A controlled by the SVID PMBus or SVID. 1'b0: SVID 1'b1: PMBus

MFR_FS_VBOOT (E5h)

The MFR_FS command on Page 0 is used to set the frequency for all the rails. The MFR_VBOOT command on Page 0 is used to set the boot-up voltage for Rail A.

Command	MFR_FS_VBOOT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_FS (50kHz/LSB)								MFR_VBOOT							

Bits	Bit Name	Description
[15]	MFR_SLP_S0_FUN[2]	One enable bit in the ATOM platform of Rail A to set a new VID when SLP_S0# asserts. This bit is used combined with MFR_SLP_S0_FUN[1]. At the SLP_S0# negative edge, MFR_SLP_S0_FUN[1] = MFR_SLP_S0_FUN[2] = 1, and VID goes to the VID set by VOUT_ATOM_SLP_AST.
[14:8]	MFR_FS	Sets the operation frequency for all rails. 50kHz/LSB.
[7:0]	MFR_VBOOT	Sets the boot-up voltage for Rail A (VID format). For example, to set the output voltage at 0.9V, set E5h[7:0] = 8'h83 (5mV VID mode) or 8'h47 (10mV VID mode).

MFR_ADDR_SVID (E6h)

The MFR_ADDR_SVID command on Page 0 is used to set the SVID address for the controller.

Command	MFR_ADDR_SVID															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function			ALLCALL_CTRL		SVID ADDR OF RC				SVID ADDR OF RB				SVID ADDR OF RA			

Bits	Bit Name	Description
[15]	MFR_SLP_S0_FUN[1]	One ATOM platform enable bit of Rail A that sets a new VID when SLP_S0# asserts or deasserts. This bit is used with MFR_SLP_S0_FUN[2]. At the SLP_S0# negative edge, MFR_SLP_S0_FUN[1] = MFR_SLP_S0_FUN[2] = 1, and VID goes to the VID set by VOUT_ATOM_SLP_AST. At the SLP_S0# positive edge, MFR_SLP_S0_FUN[1] = 1, and VID goes to the VID set by VOUT_ATOM_SLP_DEAST.
[14]	MFR_SLP_S0_FUN[0]	Enable bit of shutting off the SVID interface when SLP_S0# asserts during PS4. 1'b0: disable 1'b1: enable
[13:12]	ALLCALL_CTRL	Sets the All Call address. 2'b 00: no All Call address 2'b 01: set 0Eh to be All Call address 2'b 10: set 0Fh to be All Call address 2'b 11: set both 0Eh and 0Fh to be All Call addresses
[11:8]	RAILC_SVID_ADDRESS	Set the SVID address of Rail C. 4'b 0000: Set Rail C address to 00h 4'b 0001: Set Rail C address to 01h 4'b 0010: Set Rail C address to 10h 4'b 0011: Set Rail C address to 11h
[7:4]	RAILB_SVID_ADDRESS	Set the SVID address of Rail B. 4'b 0000: set Rail B address to 00h 4'b 0001: set Rail B address to 01h 4'b 0010: set Rail B address to 10h 4'b 0011: set Rail B address to 11h
[3:0]	RAILA_SVID_ADDRESS	Sets the SVID address of Rail A. 4'b 0000: set Rail A address to 00h 4'b 0001: set Rail A address to 01h 4'b 0010: set Rail A address to 10h 4'b 0011: set Rail A address to 11h

VFB_TRIM_DCLL (E7h)

The VFB_TRIM_DCLL command on Page 0 is used to record the VFB buffer trim without the IDROOP and DC load line of Rail A.

Command	VFB_TRIM_DCLL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	VFB buffer trim without IDROOP						DC load line, 0.1mΩ/LSB							

Bits	Bit Name	Description
[15:14]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[13:8]	VFB buffer trim without IDROOP	Records the Rail A VFB buffer trim without IDROOP.
[7:0]	DC load line	Records the Rail A DC load line. 0.1mΩ/LSB.

TEMPERATURE_GAIN_OFFSET (E8h)

The TEMPERATURE_GAIN_OFFSET command on Page 0 is used to set the gain and offset of the temperature sense.

Command	TEMPERATURE_GAIN_OFFSET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_TEMP_GAIN								MFR_TEMP_OFFSET							

Bits	Bit Name	Description
[15:8]	MFR_TEMP_GAIN	Sets the temperature (T(°C)) and temperature sense voltage (V _{TEMP_SENSE}) relationship. T(°C) = A x V _{TEMP_SENSE} + B, where A is MFR_TEMP_GAIN/0.8, and B is MFR_TEMP_OFFSET.
[7:0]	MFR_TEMP_OFFSET	The offset is used to set the offset of the temperature sense. Signed value, 1°C/LSB. For example, to set MFR_TEMP_OFFSET as -2°C, set MFR_TEMP_OFFSET to 8'hFE.

MFR_CUR_GAIN (E9h)

The MFR_CUR_GAIN command on Page 0 is used to set the per-phase current sense gain of Rail A. Calculate I_{READ} with Equation (11):

$$I_{READ} = \frac{I_{CS} * K_{CS} * R_{CS} + 1.23}{32 * MFR_CUR_GAIN} * 1023 - MFR_CUR_OFFSET \quad (11)$$

Where K_{CS} is in µA/A, and R_{CS} is in Ω.

Command	MFR_CUR_GAIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_CUR_GAIN									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_CUR_GAIN	Sets the gain of the per-phase current sense of Rail A. MFR_CUR_GAIN is used to calculate the current from per-phase current sample results.

MFR_CUR_OFFSET (EAh)

The MFR_CUR_OFFSET command on Page 0 is used to set the offset for the Rail A 1.23V bias voltage of the per-phase current sense.

Command	MFR_CUR_OFFSET							
Format	signed binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_CUR_OFFSET							

Bits	Bit Name	Description
[7:0]	MFR_CUR_OFFSET	Sets the offset for the 1.23V bias voltage of the per-phase current sense.

MFR_CS_OFFSET1_2 (EBh)

The MFR_CS_OFFSET1_2 command on Page 0 is used to set the phase 1/2 current bias for thermal offset.

Command	MFR_CS_OFFSET1_2															
Format	signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_CS_OFFSET1								MFR_CS_OFFSET2							

Bits	Bit Name	Description
[15:8]	MFR_CS_OFFSET1	Sets the CS1 offset in the current balance loop. 3.125mV/LSB.
[7:0]	MFR_CS_OFFSET2	Sets the CS2 offset in the current balance loop. 3.125mV/LSB.

MFR_CS_OFFSET3_4 (ECh)

The MFR_CS_OFFSET3_4 command on Page 0 is used to set the phase 3/4 current bias for thermal offset.

Command	MFR_CS_OFFSET3_4															
Format	signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_CS_OFFSET3								MFR_CS_OFFSET4							

Bits	Bit Name	Description
[15:8]	MFR_CS_OFFSET3	Sets the CS3 offset in the current balance loop. 3.125mV/LSB.
[7:0]	MFR_CS_OFFSET4	Sets the CS4 offset in the current balance loop. 3.125mV/LSB.

MFR_CS_OFFSET5_6 (EDh)

The MFR_CS_OFFSET5_6 command on Page 0 is used to set the phase 5/6 current bias for thermal offset.

Command	MFR_CS_OFFSET5_6															
Format	signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_CS_OFFSET5								MFR_CS_OFFSET6							

Bits	Bit Name	Description
[15:8]	MFR_CS_OFFSET5	Sets the CS5 offset in the current balance loop. 3.125mV/LSB.
[7:0]	MFR_CS_OFFSET6	Sets the CS6 offset in the current balance loop. 3.125mV/LSB.

MFR_OCP_SET_LEVEL (EEh)

The MFR_OCP_SET_LEVEL command on Page 0 is used to set the Rail A OC limit level and the OCP delay time for the three rails.

Command	MFR_OCP_SET_DELAYTIME, MFR_OCP_SET_LEVEL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	MFR_OCP_SET_DELAYTIME						X	MFR_OCP_SET_LEVEL						

Bits	Bit Name	Description
[15:14]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[13:8]	MFR_OCP_SET_DELAY TIME	Sets the average OCP delay time for the three rails. 20μs/LSB.
[7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6:0]	MFR_OCP_SET_LEVEL	Sets the Rail A over-current limit value (1A/LSB). The total OCP limit is set at [6:0]*phase num, which is compared with READ_IOUT(8Ch)/4.

OCP_LIMIT_ICC_MAX (EFh)

The OCP_DA_LIMIT on Page 0 is used to set the single-phase valley current limit of Rail A. The MFR_ICC_MAX command on Page 0 is used to set the ICCMAX of Rail A.

Command	OCP_LIMIT_ICC_MAX															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OCP_DA_LIMIT								MFR_ICC_MAX							

Bits	Bit Name	Description
[15:8]	OCP_DA_LIMIT	Sets the valley limitation level of the current sense (CS) of a single phase for Rail A. 10mV/LSB. The MP2949A will not latch when it reaches the limit and usually ends in UVP.
[7:0]	MFR_ICC_MAX	Sets the ICCMAX for Rail A. 1A/LSB. 00h indicates that this value is not programmed and the platform will not boot.

MFR_VOUT_CMPS_MAX (F0h)

The MFR_VOUT_CMPS_MAX command on Page 0 is the maximum level of V_{OUT} compensation of all rails.

Command	MFR_VOUT_CMPS_MAX							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_VOUT_CMPS_MAX							

Bits	Bit Name	Description
[7:0]	MFR_VOUT_CMPS_MAX	Sets all rails' max level of V _{OUT} compensation. 0.34mV/LSB.

UVP_OVP_OCP_MODE (F1h)

The MFR_PLATFORM_TIME command on Page 0 is used to set the platform time for Rail A. The command MFR_UVP_OVP_OCP_SET_MODE sets the UV/OV/OC protection mode for Rail A.

Command	UVP_OVP_OCP_MODE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_PLATFORM TIME											

Bits	Bit Name	Description
[15:12]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[11:6]	MFR_PLATFORM_TIME	Sets the period after VID has added the rising step and before VID starts to subtract the rising step of Rail A. 0.5µs/LSB.
[5:4]	MFR_UVP_SET_MODE	Sets the Rail A UVP mode. 2'b00: no action 2'b01: latch 2'b01: hiccup 2'b11: retry six times and then latch off
[3:2]	MFR_OVP_SET_MODE	Sets the Rail A OVP2 mode. 2'b00: no action 2'b01: latch 2'b01: hiccup 2'b11: retry six times and then latch off
[1:0]	MFR_OCP_SET_MODE	Sets the Rail A OCP mode. 2'b00: no action 2'b01: latch 2'b01: hiccup 2'b11: retry six times and then latch off

MFR_OTP_SET (F2h)

The MFR_OTP_SET command on Page 0 is used to set the OTP level for the VR.

Command	MFR_OTP_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_OTP_LIMIT								X	MFR_OTP_HYS						

Bits	Bit Name	Description
[15:8]	MFR_OTP_LIMIT	Sets the OTP limit. When the junction temperature monitored on TEMP is higher than OTP_LIMIT, the VR shuts off and disables the output. 1°C/LSB.
[7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6:0]	MFR_OTP_HYS	Sets the temperature hysteresis of OTP if OTP is in no-latch mode, when the junction temperature monitored on TEMP is lower than MFR_OTP_LIMIT - MFR_OTP_HYS, the PWM initiates a soft start as it would during a normal power-on. 1°C/LSB.

MFR_TEMP_MAX (F3h)

The MFR_TEMP_MAX command on Page 0 is used to set the max temperature the platform supports and the level VRHOT# asserts.

Command	MFR_TEMP_MAX							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_TEMP_MAX							

Bits	Bit Name	Description
[7:0]	MFR_TEMP_MAX	Sets the over-temperature warning limit setting. VRHOT# asserts when the sensed temperature reaches this threshold. 1°C/LSB.

MFR_FIXED_OVP_SET (F6h)

The MFR_FIXED_OVP_SET command on Page 0 is used to set the Rail A OVP1 level.

Command	MFR_FIXED_OVP_SET							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_FIXED_OVP_SET							

Bits	Bit Name	Description
[7]	Bit[7]	Sets the Rail A OVP1 level. 1'b0: OVP1 limitation is set at 0V 1'b1: OVP1 limitation depends on bit[6:0]
[6:0]	MFR_FIXED_OVP_SET	Sets the Rail A OVP1 level. Once the sensed VOUT (VDIFF) is over this level, the VR is protected. 20mV/LSB. For example, to set the OVP1 level at 1.92V, set F6h = 8'hB0 for the 1/2 buffer on the remote sense.

MFR_OVP_UVP_SET (F7h)

The MFR_OVP_UVP_SET command on Page 0 is used to set the delay time of OVP2 and UVP for all the rails.

Command	MFR_OVP_UVP_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	OVP2 DELAYTIME (200ns/LSB)						UVP DELAYTIME (20µs/LSB)					

Bits	Bit Name	Description
[15:12]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[11:6]	OVP2 DELAYTIME	Sets the OVP2 delay time for the three rails. 200ns/LSB.
[5:0]	UVP DELAYTIME	Sets the UVP delay time for the three rails. 20µs/LSB.

MFR_FILTER_SET (F9h)

The MFR_FILTER_SET on Page 0 is used to set the parameters of the VID filter and slow the slew rate for Rail A.

Command	MFR_FILTER_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_IVID_VALID_WAITTIME (100ns/LSB)												SLOW_SR_SEL			

Bits	Bit Name	Description
[15:8]	MFR_IVID_VALID_WAITTIME	Sets the IVID phase shedding delay time. 100ns/LSB.
[7]	MFR_DAC_CMP_EN	Enable bit of DAC_CMP_FILTER from the analog of Rail A, which is used to filter the VID_DAC output until the filtered VID_DAC output level equals the VID_DAC output when SetVID_down is interrupted by SetVID_up. 1'b0: disable 1'b1: enable
[6]	MFR_VID_FILTER_EN	Enable bit of the VID filter for Rail A, which is the VID_DAC output filter for SetVID_fast/slow_down transitions. There is no VID filter when VID is up or VID is down by decay. Set PS4 CMD. 1'b0: disable 1'b1: enable
[5:4]	MFR_VID_FILTER	Sets Rail A VID_DAC output filter. 2'b00: 1μs added filter at VID ramping down or steady V _{OUT} 2'b01: 3μs added filter at VID ramping down or steady V _{OUT} 2'b10: 5μs added filter at VID ramping down or steady V _{OUT} 2'b11: 7μs added filter at VID ramping down or steady V _{OUT}
[3:0]	SLOW_SR_SEL	Selection bit of the slew rate when Rail A receives the SetVID_Slow command. 4'b1xxx: 1/16 of the fast slew rate 4'b01xx: 1/8 of the fast slew rate 4'b001x: 1/4 of the fast slew rate 4'b0001: 1/2 of the fast slew rate

MFR_TRANS_FAST (FAh)

The MFR_TRANS_FAST command on Page 0 is used to set the Rail A reference fast slew rate when Rail A receives the SetVID_Fast_Up command. The REF down slew rate is set by the FDh register. Figure 21 shows the definition of the slew rate of VREF up and down (5mV/LSB). VID_STEP: FAh[7:6], VID_SR_CNT: FAh[5:0], ALERT_STEP_NUM: FDh[13:12], ALERT_SR_CNT: FDh[5:0].

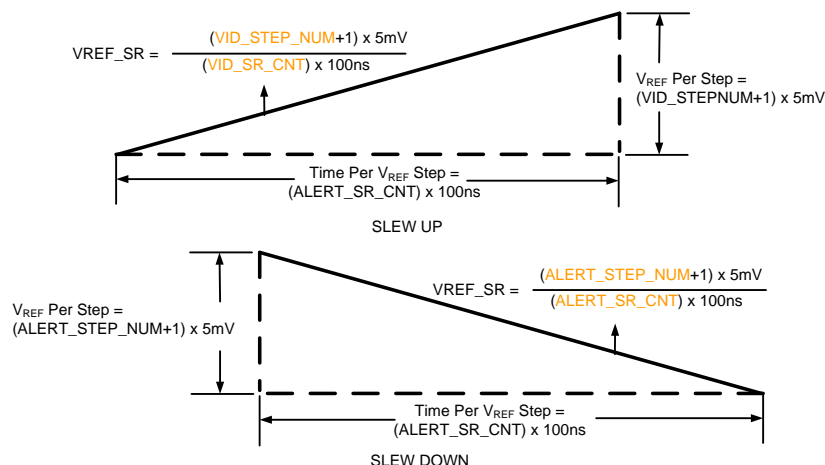


Figure 21: Slew Rate Definition

Normal slew rate = ([7:6] + 1) * 5mV / ([5:0] * 100ns) * 10³ (mV/μs), in 5mV mode.

Normal slew rate = ([7:6] + 1) * 10mV / ([5:0] * 100ns) * 10³ (mV/μs), in 10mV mode.

Command	MFR_TRANS_FAST															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
[15:14]	VID_STEP_DECAY	Sets the Rail A reference minus the step during decay. The step = 2 * bit[15:14] + 1.
[13]	SLP_S0_POS	Selection bit of the Rail A slew rate at the SLP_S0# positive edge at the ATOM platform. 1'b0: slow slew rate 1'b1: fast slew rate
[12]	SLP_S0_NEG	Selection bit of the Rail A slew rate at the SLP_S0# negative edge at the ATOM platform. 1'b0: slow slew rate 1'b1: fast slew rate
[11]	VID_SUBTRACT	Selection bit of the Rail A slew rate when the reference removes the additional rising step. 1'b0: 1/4 of the fast slew rate 1'b1: 1/8 of the fast slew rate
[10:8]	MORE_RISING_STEP	Sets the number of additional rising steps of Rail A after the VID reaches the target to increase the output voltage. Rising step = [10:8] * 2 + 1 in 5mV mode Rising step = [10:8] in 10mV mode
[7:6]	VID_STEP_NUM	Sets the Rail A reference step at one VID_SR_CNT period when slewing up. The step is equal to DEC([7:6]) + 1.
[5:0]	VID_SR_CNT	Sets the time length of Rail A that VREF changes once. 100ns/LSB.

MFR_EN_DLY (FBh)

The MFR_EN_DLY command on Page 0 is used to set the Rail A EN delay time. MFR_EN_FILTER_TIME is used to set the EN filter time for the three rails.

Command	MFR_EN_DLY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	MFR_EN_FILTER_TIME				MFR_EN_DLY						

Bits	Bit Name	Description
[15:11]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[10:7]	MFR_EN_FILTER_TIME	It is used to set the synchronized EN pulse length to be high for EN start-up or EN re-start-up for the three rails. 100µs/LS.
[6:0]	MFR_EN_DLY	Sets the delay for Rail A to wait to output power after FBh[10:7] (on Page 0) passes, and there is no VIN or temp fault. 20µs/LSB. This is the second delay for the start, and it is also the delay of hiccup, retry, and PMBus off and on.

MFR_IMON_SVID (FCh)

The MFR_IMON_SVID command on Page 0 is used to set the gain and offset of the Rail A I_{OUT} report from the VR to the SVID processor. R_{imon} can be calculated with Equation (12):

$$R_{imon} = \frac{1.6 \times 8 \times 32}{11 \times K_{cs} \times MFR_ICC_MAX} \quad (12)$$

Where K_{CS} is the Intelli-Phase current sense gain (in µA/A).

Command	MFR_IMON_SVID															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_IMON_SVID_OFFSET								MFR_IMON_SVID_GAIN						

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:8]	MFR_IMON_SVID_OFFSET	Sets the Rail A I _{OUT} SVID report offset, which is added to the value directly to the SVID I _{OUT} report register (15h). The default value is 0. Bit[14] is the sign bit. If setting the offset to -1, set [14:8] = 7'h7F If setting the offset to -2, set [14:8] = 7'h7E
[7:0]	MFR_IMON_SVID_GAIN	Sets the gain of the Rail A I _{OUT} SVID report. The default value is 128.

MFR_ALT_SET (FDh)

The MFR_ALT_SET command on Page 0 is used to set the Rail A alert timing.

Slew rate of the alert reference: $([13:12] + 1) * 5\text{mV} / ([5:0] * 100\text{ns}) * 10^3 \text{ (mV/}\mu\text{s)}$, in 5mV mode.

Slew rate of the alert reference: $([13:12] + 1) * 10\text{mV} / ([5:0] * 100\text{ns}) * 10^3 \text{ (mV/}\mu\text{s)}$, in 10mV mode.

Command	MFR_ALT_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
[15:14]	ALERT_STEP_DECAY	Sets the VID decreasing step of Rail A during decay. The step is equal to $2 * \text{DEC} ([15:14] + 1)$.
[13:12]	ALERT_STEP_NUM	Sets the decreasing step for Rail A at a non-decay VID. The step is set to $\text{DEC} ([13:12] + 1)$.
[11]	SET_DACAY_FINISH	Selection bit for Rail A of when to pull the VR_settle signal high. 1'b0: waits for a set pulse after the decay is finished to pull the VR_settle signal high. 1'b1: does not wait for a set pulse after the decay is finished to pull the VR_settle signal high.
[10:6]	ALERT_DELAY_TIME	Sets the Rail A delay time to pull the VR_settle signal high after the alert reference reaches the target VID. 100ns/LSB.
[5:0]	ALERT_SR_CNT	Sets the Rail A time length of the alert reference changing one step. 100ns/LSB.

CLEAR_EEPROM_FAULTS (FEh)

The CLEAR_EEPROM_FAULTS command is used to clear the EEPROM fault bits. The VR starts ramping and outputs power if no other protection exists. This command is write only. There is no data byte for this command.

PAGE 1 REGISTER MAP

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor through only one physical address for the three rails and test mode.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w
Function	X	X	X	X	X	X	PAGE	

Bits	Bit Name	Description
[7:2]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[1:0]	PAGE	2'b00: Page 0, all commands address Rail A 2'b01: Page 1, all commands address Rail B 2'b10: Page 2, all commands address Rail C Others: ineffective input

OPERATION (01h)

The OPERATION command on Page 1 is used to turn the Rail B output on or off in conjunction with input from EN. OPERATION is also used to set the output voltage to the upper or lower margin voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of EN instructs the device to change to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OPERATION_MODE							

Bits	Bit Name	Description
[7:0]	OPERATION_MODE	Sets the operation mode for Rail B. 7'b00xxxxx: immediate off 7'b1000xxx: normal on 7'b1001xxx: margin low 7'b1010xxx: margin high 7'b100101xx: margin low, ignore fault (ignore UV) 7'b101001xx: margin high, ignore fault (ignore OV2) The value of "x" does not matter.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set on Rail B. This command clears all bits in all status registers simultaneously. This command is write only. There is no data byte for this command.

CLEAR_LAST_FAULT (08h)

See the Page 0 LAST_FAULT_BLOCK (07h) section on page 33.

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus device to copy the Page 0 ~ Page 2 contents (not including read-only registers) of the operating memory to the matching locations in the MTP, regardless of the current PMBus register page. This command can be used while the device is outputting power. This command is write only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBus device to copy the Page 0 ~ Page 2 contents of the MTP to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the user store. Any items in the user store that do not have matching locations in the operating memory are ignored. It is *not* permitted to use this command while the device is outputting power unless MFR_EEPROM_COPY_EN (register 1Dh[1] on Page 0) is set to 1. This command is write only. There is no data byte for this command.

IDROOP_CTRL (1Bh)

The IDROOP_CTRL command on Page 1 is used to set the IDROOP DC gain for Rail B.

Command	IDROOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X		IDROOP_DC_SET			

Bits	Bit Name	Description																																				
[15:5]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.																																				
[4]	IDROOP_EN	Selection bit of the AC droop of Rail B. 1'b0: enable DC droop 1'b1: enable AC droop																																				
[3:0]	IDROOP_DC_SET	Sets the Rail B IDROOP DC gain to set the digital load line gain. The default value of 'Idroop_set' is 1 h.																																				
		<table><tr><th>Idroop_set[3:0]</th><th>Gain</th><th>Idroop_set[3:0]</th><th>Gain</th></tr><tr><td>0 h</td><td>0</td><td>8 h</td><td>11/8 * 1/8</td></tr><tr><td>1 h</td><td>4/8 * 1/8</td><td>9 h</td><td>12/8 * 1/8</td></tr><tr><td>2 h</td><td>5/8 * 1/8</td><td>A h</td><td>13/8 * 1/8</td></tr><tr><td>3 h</td><td>6/8 * 1/8</td><td>B h</td><td>14/8 * 1/8</td></tr><tr><td>4 h</td><td>7/8 * 1/8</td><td>C h</td><td>15/8 * 1/8</td></tr><tr><td>5 h</td><td>8/8 * 1/8</td><td>D h</td><td>16/8 * 1/8</td></tr><tr><td>6 h</td><td>9/8 * 1/8</td><td>E h</td><td>17/8 * 1/8</td></tr><tr><td>7 h</td><td>10/8 * 1/8</td><td>F h</td><td>18/8 * 1/8</td></tr></table>	Idroop_set[3:0]	Gain	Idroop_set[3:0]	Gain	0 h	0	8 h	11/8 * 1/8	1 h	4/8 * 1/8	9 h	12/8 * 1/8	2 h	5/8 * 1/8	A h	13/8 * 1/8	3 h	6/8 * 1/8	B h	14/8 * 1/8	4 h	7/8 * 1/8	C h	15/8 * 1/8	5 h	8/8 * 1/8	D h	16/8 * 1/8	6 h	9/8 * 1/8	E h	17/8 * 1/8	7 h	10/8 * 1/8	F h	18/8 * 1/8
		Idroop_set[3:0]	Gain	Idroop_set[3:0]	Gain																																	
		0 h	0	8 h	11/8 * 1/8																																	
		1 h	4/8 * 1/8	9 h	12/8 * 1/8																																	
		2 h	5/8 * 1/8	A h	13/8 * 1/8																																	
		3 h	6/8 * 1/8	B h	14/8 * 1/8																																	
		4 h	7/8 * 1/8	C h	15/8 * 1/8																																	
		5 h	8/8 * 1/8	D h	16/8 * 1/8																																	
		6 h	9/8 * 1/8	E h	17/8 * 1/8																																	
7 h	10/8 * 1/8	F h	18/8 * 1/8																																			

VOUT_COMMAND (21h)

The VOUT_COMMAND command on Page 1 set the Rail B output voltage when the PMBus controls the output.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X		VOUT_COMMAND						

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VOUT_COMMAND	Sets the Rail B reference voltage (VID_DAC output voltage) in PMBus mode. In 5mV mode (E4h[5] = 1'b1): VREF = (VID + 49) / 2 * 5mV In 10mV mode (E4h[5] = 1'b0): VREF = (VID + 19) / 2 * 10mV

MFR_VOUT_TRIM (22h)

This MFR_VOUT_TRIM command on Page 0 is used to apply a fixed offset voltage to the Rail B output voltage command value for different power states. This command is most typically used by the end user to trim the output voltage at the time the PMBus device is assembled into the end user's system.

Command	MFR_VOUT_TRIM															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	VOUT_TRIM_2_CCM				VOUT_TRIM_1_CCM				VOUT_TRIM_1_DCM			

Bits	Bit Name	Description
[15:12]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[11:8]	VOUT_TRIM_2_CCM	Applies a fixed offset voltage to the Rail B output voltage at 2-phase CCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.
[7:4]	VOUT_TRIM_1_CCM	Applies a fixed offset voltage to the Rail B output voltage at 1-phase CCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.
[3:0]	VOUT_TRIM_1_DCM	Applies a fixed offset voltage to the Rail B output voltage at 1-phase DCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.

VOUT_CAL_OFFSET (23h)

The VOUT_CAL_OFFSET command on Page 1 offers an offset VID to the Rail B target determined by VOUT_COMMAND, VOUT_MARGIN_HIGH, and VOUT_MARGIN_LOW. This command is the initial value of the Rail B SVID offset.

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VOUT_CAL_OFFSET	Sets the VID offset in PMBus mode. It is also the initial value for the SVID offset register (33h). 5mV/LSB or 10mV/LSB according to E4h[5], -80h ~ +7Fh.

MFR_VOUT_MAX (24h)

The MFR_VOUT_MAX command on Page 1 is the Rail B initial value of SVID VOUT_MAX (SVID 30h), which sets an upper limit on the VID target (not including the offset) of SVID so as to provide a safeguard against an accidental setting of the output voltage to a possibly destructive level. If an attempt is made to program the VID target higher than VOUT_MAX, the command is rejected. The PMBus VID target is not constrained by MFR_VOUT_MAX.

Command	MFR_VOUT_MAX															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	MFR_VOUT_MAX							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	MFR_VOUT_MAX	Sets an upper limit on the Rail B VID target (not including the offset) of SVID.

VOUT_MARGIN_HIGH (25h)

The VOUT_ATOM_SLP_DEAST command on Page 1 is used to set the Rail B VID target when the SLP_S0# signal deasserts on the ATOM platform. The VOUT_MARGIN_HIGH command is used to set the Rail B reference voltage (VID_DAC output voltage) at the command MARGIN HIGH state.

Command	VOUT_MARGIN_HIGH															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VOUT_ATOM_SLP_DEAST								VOUT_MARGIN_HIGH							

Bits	Bit Name	Description
[15:8]	VOUT_ATOM_SLP_DEAST	Sets the Rail B reference voltage (VID_DAC output voltage) when SLP_S0# asserts in ATOM mode.
[7:0]	VOUT_MARGIN_HIGH	Sets the Rail B reference voltage (VID_DAC output voltage) at the command MARGIN HIGH state.

VOUT_MARGIN_LOW (26h)

The VOUT_ATOM_SLP_AST command on Page 1 is used to set the Rail B VID target when the SLP_S0# signal asserts on the ATOM platform. The VOUT_MARGIN_LOW command is used to set the Rail B reference voltage (VID_DAC output voltage) at the command MARGIN LOW state.

Command	VOUT_MARGIN_LOW															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VOUT_ATOM_SLP_AST								VOUT_MARGIN_LOW							

Bits	Bit Name	Description
[15:8]	VOUT_ATOM_SLP_AST	Sets the Rail B reference voltage (VID_DAC output voltage) when SLP_S0# deasserts in ATOM mode.
[7:0]	VOUT_MARGIN_LOW	Sets the Rail B reference voltage (VID_DAC output voltage) at the command MARGIN LOW state.

MFR_IMMEDIATE_SET (2Bh)

The MFR_IMMEDIATE_SET command on Page 1 sets the Rail B slew rate, alert time, and bit[0] of STATUS1 when SVID sends VID within $\pm 2\text{LSB}$ in 5mV mode.

Command	MFR_IMMEDIATE_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:8]	MFR_IMMED_REF_STEP	Sets the VID (output reference) step when SVID sends VID within $\pm 2\text{LSB}$ in 5mV mode of Rail B.
[7:5]	MFR_IMMED_ALT_TIME	Sets the time length of the ALTER slewing one step ($\text{FD}[13:12] + 1$) when SVID sends VID within $\pm 2\text{LSB}$ in 5mV mode of Rail B. 100ns/LSB.
[4:2]	MFR_IMMED_REF_TIME	Sets the time length of the VID slewing one step ([9:8]) when SVID sends VID within $\pm 2\text{LSB}$ in 5mV mode of Rail B. 100ns/LSB.
[1]	MFR_IMMEDIATE_SVID_EN	Enable bit of Rail B to force the STATUS bit[0] to 1'b1. 1'b0: disable, STATUS bit[0] remains at 1'b0 until it settles normally. 1'b1: enable. Force STATUS bit[0] to 1'b1 when the SetVID command is received within $\pm 2\text{LSB}$.
[0]	MFR_IMMEDIATE_REF_EN	Enable bit of Rail B using bit[9:2]. 1'b0: disable 1'b1: enable

MFR_DEBUG (2Fh)

The MFR_DEBUG command on Page 1 is used to debug Rail B.

Command	MFR_DEBUG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r
Function	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X

Bits	Bit Name	Description
[15:2]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[1]	div2_en	Selects VDIFF to be above or below VREF 30mV or 15mV to trigger p30/n30. 1'b0: 30mV 1'b1: 15mV
[0]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.

IOUT_CAL_GAIN (38h)

The IOUT_CAL_GAIN command on Page 1 is used to set the Rail B PMBus I_{OUT} report (0.25A/LSB) gain and can be calculated with Equation (13):

$$\text{IOUT_CAL_GAIN} = \frac{K_{\text{CS}} * R_{\text{imon}} * 2^{15}}{32 * 1000 * k} \quad (13)$$

Where K_{CS} is the CS gain of the Intelli-Phase (in $\mu\text{A/A}$) (e.g.: MPS 86901C $K_{\text{CS}} = 10\mu\text{A/A}$), R_{imon} is the resistor connected to IMON (in k Ω), and k is a coefficient according to ICCMAX.

Command	IOUT_CAL_GAIN															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	k						IOUT_CAL_GAIN									

Bits	Bit Name	Description
[15:11]	k	$k = 1$, IOUT_CAL_GAIN[15:11] = 5'b10001, when $20\text{A} \leq \text{ICCMAX}$ $k = 2$, IOUT_CAL_GAIN[15:11] = 5'b10010, when $10\text{A} \leq \text{ICCMAX} < 20\text{A}$ $k = 4$, IOUT_CAL_GAIN[15:11] = 5'b10011, when $5\text{A} \leq \text{ICCMAX} < 10\text{A}$
[10:0]	IOUT_CAL_GAIN	Sets the Rail B PMBus I _{OUT} report gain.

IOUT_CAL_OFFSET (39h)

The IOUT_CAL_OFFSET command on Page 1 is used to set the Rail B PMBus I_{OUT} report offset.

Command	IOUT_CAL_OFFSET															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED						X	X	X	X	X	IOUT_CAL_OFFSET				

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to -1 (dec) = 11111 (bin).
[10:6]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[5:0]	IOUT_CAL_OFFSET	Signed value to set the Rail B PMBus I _{OUT} report offset. 0.5A/LSB. Default value is 0. Bit[5] is the sign bit. For example, write 1111100000111110b = F83Eh to 39h to add -1A offset on the PMBus I _{OUT} report.

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 1 is a combined register of the output voltage fault flags for Rail B.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x	x			x	x	x
Default	0	x	x	0	0	x	x	x

Bits	Bit Name	Description
[7]		OVP flag. This bit is 1 if OVP is tripped.
[6]		Reserved.
[5]		Reserved.
[4]		UVP flag. This bit is 1 if UVP is tripped.
[3]		Vout_max_warning. The value is written into PMBus 21h 25h/26h, which is larger than MFR_VOUT_MAX.
[2:0]		Reserved.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 1 is a combined register of the output current fault flags for Rail B.

Command	STATUS_IOUT							
Format	Unsigned binary							
bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x		x	x	x	x	x
Default	0	x	0	x	x	x	x	x

Bits	Bit Name	Description
[7]		OCF flag. This bit is 1 if OCF is tripped.
[6]		Reserved.
[5]		Phase current limit flag. This bit is 1 if the per-phase current limit is reached.
[4:0]		Reserved.

READ_VOUT (8Bh)

The READ_VOUT command on Page 1 is used to return the sensed VDIFF voltage of Rail B in VID format.

Command	READ_VOUT															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	X	READ_VOUT							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	READ_VOUT	Shows the sensed VDIFF voltage of Rail B in VID format.

READ_IOUT (8Ch)

The READ_IOUT command on Page 1 reflects the PMBus monitor Rail B total average output current.

Command	READ_IOUT (0.25A/LSB)															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	FIXED					READ_IOUT										

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to 11110 (bin) = -2 (dec).
[10:0]	READ_IOUT	Shows the total average output current of Rail B monitored by the PMBus. 0.25A/LSB.

READ_POUT (96h)

The READ_POUT command on Page 1 is used to monitor the Rail B output power.

Command	READ_POUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	READ_POUT								

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	READ_POUT	Shows the monitored output power of Rail B by the PMBus. 0.5W/LSB.

PS3_PS4_EXIT_DELAY (BEh)

The PS3_PS4_EXIT_DELAY command on Page 1 is used to set the time length of the VR to exit PS3/4. The format is the same as the SVID spec.

Command	PS3_PS4_EXIT_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PS3_EXIT_LATENCY_VR								PS4_EXIT_LATENCY_VR							

Bits	Bit Name	Description
[15:8]	PS3_EXIT_LATENCY_VR	Set the time length (in μs) for Rail B to exit PS3. The time length is equal to $[11:8] / 16 * 2^{\wedge} [15:12]$.
[7:0]	PS4_EXIT_LATENCY_VR	Set the time length (in μs) that VR takes to exit PS4. The time length is equal to $[3:0] / 16 * 2^{\wedge} [7:4]$.

DECAY_CFG_34H_06H (C2h)

The MUTI_VR_CONFIG command on Page 1 is the Rail B initial value of the SVID 34h register. The CAPABILITY_VR command on Page 1 is the bit mapped register, which identifies the SVID VR capabilities. The optional telemetry registers are supported.

Command	CFG_34H_06H															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MUTI_VR_CONFIG		CAPABILITY_VR							

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:8]	MUTI_VR_CONFIG	Initial value of the Rail B lower two bits of the SVID MUTI_VR_CONFIG (34h).
[7:0]	CAPABILITY_VR	Shows which of the telemetry registers Rail B supports. A 1 in any bit indicates that optional function is supported by the slave. Bit[7]: I _{OUT} /J _{OUT} format (15h) Bit[6]: temperature (17h) Bit[5]: input P (1Bh) Bit[4]: input V (1Ah) Bit[3]: input I (19h) Bit[2]: P _{OUT} (18h) Bit[1]: V _{OUT} (16h) Bit[0]: I _{OUT} (15h)

TOLERANCE_SR_FAST (C3h)

The MFR_VR_TOLERANCE command on Page 1 is used to set the Rail B output tolerance (binary format in mV). The SR_FAST_VR command on Page 1 is used to set the data register containing the Rail B fast slew rate capability of the slew rate the platform VR can sustain (binary format in mV/ μs).

Command	TOLERANCE_SR_FAST															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_VR_TOLERANCE								SR_FAST_VR							

Bits	Bit Name	Description
[15:8]	MFR_VR_TOLERANCE	Shows the Rail B output tolerance. 1mV/LSB.
[7:0]	SR_FAST_VR	Shows the fast slew rate that Rail B supports. 1mV/ μs per LSB.

MFR_VOUT_MAX_9BIT (C4h)

The MFR_VOUT_MAX_9BIT command on Page 1 is used to set the Rail B upper limit of VID + OFFSET. In PMBus mode, if VID + OFFSET is higher than this limit, the command is acknowledged, and the output is latched at this limit. In SVID mode, if VID + OFFSET is higher this limit, this command is rejected, and the output holds the voltage before the command.

Command	MFR_VOUT_MAX_9BIT															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	MFR_VOUT_MAX_9BIT								

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	MFR_VOUT_MAX_9BIT	Sets the Rail B upper limit of VID + OFFSET.

IVID2_1_I_DEF (C5h)

The iver2_i_def command on Page 1 is the default value of the Rail B maximum current (1A/bit) expected when VID is set as IVID2 - VID ≥ VID > IVID3 - VID. The iver1_i_def command on Page 1 is the Rail B default value of the maximum current (1A/bit) expected when VID is set as IVID1 - VID ≥ VID > IVID2 - VID.

Command	IVID2_1_I_DEF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Ivid2_i_def								Ivid1_i_def							

Bits	Bit Name	Description
[15:8]	iver2_i_def	Sets the Rail B default value of the maximum current expected when VID is set as IVID2 - VID ≥ VID > IVID3 - VID. 1A/LSB.
[7:0]	iver1_i_def	Sets the Rail B default value of the maximum current expected when VID is set as IVID1 - VID ≥ VID > IVID2 - VID. 1A/LSB.

PIN_MAX_IVID3_I_DEF (C6h)

The IVID3_I_DEF command on Page 1 is the default value of the Rail B maximum current (1A/bit) expected when VID is set as IVID3 - VID ≥ VID.

Command	PIN_MAX_IVID3_I_DEF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	Ivid3_i_def (1A/LSB)							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	Ivid3_i_def	Sets the Rail B default value of the maximum current expected when VID is set as IVID3 - VID ≥ VID. 1A/LSB.

DC_CTRL_ADP_CTRL (CCh)

The command DC_CTRL_ADP_CTRL on Page 1 is used to hold the current balance, hold the DC loop, and exit APS when a dynamic case occurs for Rail B.

Command	DC_CTRL_ADP_CTRL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	MFR_DC_CTRL										DELAY_TIME_SET			

Bits	Bit Name	Description
[15:14]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[13]	MFR_DC_CTRL[3]	Holds the Rail B DC loop for a given time, CBh[14:11], when the frequency is lower than that set by CFh[8:0], and VID is lower than that set by CBh[7:0] under PS0/PS1 (related register in Page 0). 1'b1: hold DC loop if CCh[10] = 1, enable DC loop if CCh[10] = 0 1'b0: enable DC loop if CCh[10] = 1, enable DC loop if CCh[10] = 0
[12]	MFR_DC_CTRL[2]	Enable bit for Rail B to hold the DC calibration during the load transient. 1'b0: disable 1'b1: enable
[11]	MFR_DC_CTRL[1]	Enable bit for Rail B to hold the DC calibration during Set_PS, decay, and SetVID_Fast/Slow. 1'b0: disable 1'b1: enable
[10]	MFR_DC_CTRL[0]	Enable bit for Rail B to hold the DC calibration when the PWM frequency is lower than that set by CFh[8:0] or the PWM frequency is higher than that set by CDh[13:6] during CCM. 1'b0: disable 1'b1: enable
[9]	MFR_ADP_OC_EXIT_EN	Enable bit for Rail B for 1-phase CCM/DCM to exit and enter full-phase when per-phase over-current occurs on the rail. 1'b0: disable 1'b1: enable
[8]	MFR_ADP_PSI_BYPASS	Disables the Rail B Set_PS command when auto-phase shedding is enabled (not including IVID). 1'b0: enable 1'b1: disable
[7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6]	MFR_DYNAMIC_FLT[6]	Enable bit of Rail B to exit APS and hold the current balance during the load transient. 1'b0: disable 1'b1: enable
[5]	MFR_DYNAMIC_FLT[5]	Enable bit of Rail B to exit APS and hold current balance when Rail A receives the SetVID_Fast/Slow and decay commands. 1'b0: disable 1'b1: enable
[4]	MFR_DYNAMIC_FLT[4]	Enable bit of Rail B to exit APS and hold current balance when the Rail A PWM frequency is lower or higher than the setting threshold. 1'b0: disable 1'b1: enable
[3:0]	DELAY_TIME_SET	Sets the delay time for Rail B to enable the current balance after the load transient. 20µs/LSB.

HF_PFM_DISCHG_NUM (CDh)

The DISCHG_NUM command on Page 1 is used to set the slope ramp discharge MOSFET number of Rail B.

Command	HF_PFM_SLP_DISCHG															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	X	X	DISCHG_NUM		

Bits	Bit Name	Description
[15:3]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[2:0]	DISCHG_NUM	Sets the Rail B internal slope ramp discharge MOSFET number.

MFR_TRIM_2_1_DCM (DEh)

The MFR_TRIM_2_1_DCM command on Page 1 is used to trim the Rail B output voltage during 1-phase ~ 2-phase CCM and 1-phase DCM.

Command	MFR_TRIM_2_1_DCM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_TRIM_2					MFR_TRIM_1					MFR_TRIM_DCM				

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:10]	MFR_TRIM_2	Sets the Rail B V_{OUT} trim for 2-phase CCM operation. 2.73mV/LSB.
[9:5]	MFR_TRIM_1	Sets the Rail B V_{OUT} trim for 1-phase CCM operation. 2.73mV/LSB.
[4:0]	MFR_TRIM_DCM	Sets the Rail B V_{OUT} trim for 1-phase DCM operation. 2.73mV/LSB.

MFR_CB_SATU_PI (E2h)

The MFR_CB_PI command on Page 1 is used to set the PI value for the current balance of Rail B.

Command	MFR_CB_SATU_PI															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	MFR_CB_PI							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	MFR_CB_PI	Sets the Rail B PI parameter value for the current balance.

VTRIM_STEP_VCAL_PI (E3h)

The MFR_VCAL_PI command on Page 1 is used to set the Rail B PI value for DC calibration.

Command	VTRIM_STEP_VCAL_PI															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	MFR_VCAL_PI						

Bits	Bit Name	Description
[15:7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6:0]	MFR_VCICAL_PI	Sets the PI parameter for DC loop calibration for Rail B.

MFR_VR_CONFIG (E4h)

The MFR_VR_CONFIG command on Page 1 is used to enable the function of Rail B, such as DC loop calibration, auto-phase shedding, etc.

Command	MFR_VR_CONFIG															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X												
Bits	Bit Name		Description													
[15:12]	RESERVED		Unused. X indicates that writes are ignored and always read as 0.													
[11]	MFR_PMBUS_SR_SEL		Selection bit of Rail B for the VID slew rate when the PMBus controls V _{OUT} . 1b'0: V _{OUT} changes with a fast slew rate when the PMBus controls V _{OUT} . 1b'1: V _{OUT} changes with a slow slew rate when the PMBus controls V _{OUT} .													
[10]	DC_LOOP_DCM_EN		Enable bit for Rail B DC calibration during PS2. Only active when DC_LOOP_EN is enabled. 1b'0: disable 1b'1: enable when bit[10] = 1													
[9]	DC_LOOP_EN		Enable bit for Rail B DC calibration. 1b'0: disable 1b'1: enable DC calibration in CCM. Must enable bit[11] for PS2 DC calibration.													
[8]	PMBUS_PS_EN		Enable bit for PMBus to control the power state of Rail B in PMBus mode. 1'b0: disable 1'b1: enable													
[7:6]	PMBUS_PS		Sets the Rail B power state when the PMBus controls the power state. 2'b00: PS0 2'b01: PS1 2'b10: PS2 2'b11: PS3													
[5]	TON_REDUCTION_DCM_EN		Enable bit of Rail B to reduce the PS2 on time to 75% of that in PS0. 1'b0: disable 1'b1: enable													
[4]	VID_STEP		Selection bit of the VID step for Rail B. 1'b1: 5mV/LSB 1'b0: 10mV/LSB													
[3]	IPHASE_BALNCE_EN		Enable bit of the Rail B current balance. 1'b0: disable 1'b1: enable													
[2]	APS_EN		Enable bit of the Rail B auto-phase shedding function. 1'b0: disable 1'b1: enable													
[1]	IVID_EN		Enable bit of the Rail B IVID function. 1'b0: disable 1'b1: enable													
[0]	PMBUS_MODE_SEL		Selection bit of Rail B controlled by the PMBus or SVID. 1'b0: SVID 1'b1: PMBus													

MFR_FS_VBOOT (E5h)

The MFR_FS_VBOOT command on Page 1 is used to set the boot-up voltage for Rail B.

Command	MFR_FS_VBOOT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	MFR_VBOOT							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	MFR_VBOOT	Sets the boot-up voltage for Rail B (VID format). For example, to set the output voltage at 0.9V, set E5h [7:0] = 8'h83 (5mV VID mode) or 8'h47 (10mV VID mode).

VFB_TRIM_DCLL (E7h)

The VFB_TRIM_DCLL command on Page 1 is used to record the VFB buffer trim without the IDROOP and DC load line of Rail B.

Command	VFB_TRIM_DCLL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	VFB buffer trim without IDROOP						DC load line, 0.1mΩ/LSB							

Bits	Bit Name	Description
[15:14]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[13:8]	VFB buffer trim without IDROOP	Records the Rail B VFB buffer trim without IDROOP.
[7:0]	DC load line	Records the Rail B DC load line. 0.1mΩ/LSB

MFR_CUR_GAIN (E9h)

The MFR_CUR_GAIN command on Page 1 is used to set the per-phase current sense gain of Rail B. Calculate I_{READ} with Equation (14):

$$I_{READ} = \frac{I_{CS} * K_{CS} * R_{CS} + 1.23}{32 * MFR_CUR_GAIN} * 1023 - MFR_CUR_OFFSET \quad (14)$$

Where K_{CS} is in $\mu A/A$, and R_{CS} is in Ω .

Command	MFR_CUR_GAIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_CUR_GAIN									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_CUR_GAIN	Sets the gain of the per-phase current sense of Rail B. MFR_CUR_GAIN is used to calculate the current from the per-phase current sample results.

MFR_CUR_OFFSET (EAh)

The MFR_CUR_OFFSET command on Page 1 is used to set the offset for the Rail B 1.23V bias voltage of the per-phase current sense.

Command	MFR_CUR_OFFSET							
Format	signed binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_CUR_OFFSET							

Bits	Bit Name	Description
[7:0]	MFR_CUR_OFFSET	Sets the offset for the 1.23V bias voltage of the per-phase current sense.

MFR_OCP_SET_LEVEL (EEh)

The MFR_OCP_SET_LEVEL command on Page 1 is used to set the Rail B OC limit level.

Command	MFR_OCP_SET_DELAYTIME, MFR_OCP_SET_LEVEL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	MFR_OCP_SET_LEVEL						

Bits	Bit Name	Description
[15:7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6:0]	MFR_OCP_SET_LEVEL	Sets the Rail B over-current limit value (1A/LSB). The total OCP limit is set at [6:0]*phase num, which is compared with READ_IOUT(8Ch)/4.

OCP_LIMIT_ICC_MAX (EFh)

The OCP_DA_LIMIT on Page 1 is use to set the single-phase valley current limit of Rail B. The MFR_ICC_MAX command on Page 1 is used to set the ICCMAX of Rail B.

Command	OCP_LIMIT_ICC_MAX															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OCP_DA_LIMIT								MFR_ICC_MAX							

Bits	Bit Name	Description
[15:8]	OCP_DA_LIMIT	Sets the valley limitation level of the current sense (CS) of a single phase for Rail B. 10mV/LSB. The MP2949A will not latch when it reaches the limit and usually ends in UVP.
[7:0]	MFR_ICC_MAX	Sets the ICCMAX for Rail B. 1A/LSB. 00h indicates that this value is not programmed and the platform will not boot.

UVP_OVP_OCP_MODE (F1h)

The UVP_OVP_OCP_MODE command on Page 1 is used to set the platform time and the UV/OV/OC protection modes for Rail B.

Command	UVP_OVP_OCP_MODE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_PLATFORM TIME											

Bits	Bit Name	Description
[15:12]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[11:6]	MFR_PLATFORM_TIME	Sets the period after VID has added the rising step and before VID starts to subtract the rising step of Rail B. 0.5µs/LSB.
[5:4]	MFR_UVP_SET_MODE	Sets the Rail B UVP mode. 2'b00: no action 2'b01: latch 2'b01: hiccup 2'b11: retry six times and then latch off
[3:2]	MFR_OVP_SET_MODE	Sets the Rail B OVP2 mode. 2'b00: no action 2'b01: latch 2'b01: hiccup 2'b11: retry six times and then latch off
[1:0]	MFR_OCP_SET_MODE	Sets the Rail B OCP mode. 2'b00: no action 2'b01: latch 2'b01: hiccup 2'b11: retry six times and then latch off

MFR_FIXED_OVP_SET (F6h)

The MFR_FIXED_OVP_SET command on Page 1 is used to set the Rail B OVP1 level.

Command	MFR_FIXED_OVP_SET							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_FIXED_OVP_SET							

Bits	Bit Name	Description
[7]	Bit[7]	Sets the Rail B OVP1 level. 1'b0: OVP1 limitation is set at 0V. 1'b1: OVP1 limitation depends on bit[6:0].
[6:0]	MFR_FIXED_OVP_SET	Sets the Rail B OVP1 level. Once the sensed V_{OUT} (VDIFF) is over this level, the VR is protected. 20mV/LSB. For example, to set the OVP1 level at 1.92V, set F6h = 8'hB0 for the 1/2 buffer on the remote sense.

MFR_FILTER_SET (F9h)

The MFR_FILTER_SET on Page 1 is used to set the parameters of the VID filter and slow the slew rate for Rail B.

Command	MFR_FILTER_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X			MFR_VID_FILTER		SLOW_SR_SEL			

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7]	MFR_DAC_CMP_EN	Enable bit of DAC_CMP_FILTER from the analog of Rail B, which is used to filter the VID_DAC output until the filtered VID_DAC output level equals the VID_DAC output when SetVID_down is interrupted by SetVID_up. 1'b0: disable 1'b1: enable
[6]	MFR_VID_FILTER_EN	Enable bit of the VID filter for Rail B, which is the VID_DAC output filter for SetVID_fast/slow_down transitions. There is no VID filter when VID is up or VID is down by decay. Set PS4 CMD. 1'b0: disable 1'b1: enable
[5:4]	MFR_VID_FILTER	Sets the Rail B VID_DAC output filter. 2'b00: 1μs added filter at VID ramping down or steady V _{OUT} 2'b01: 3μs added filter at VID ramping down or steady V _{OUT} 2'b10: 5μs added filter at VID ramping down or steady V _{OUT} 2'b11: 7μs added filter at VID ramping down or steady V _{OUT}
[3:0]	SLOW_SR_SEL	Selection bit of the slew rate when Rail B receives the SetVID_Slow command. 4'b1xxx: 1/16 of the fast slew rate 4'b01xx: 1/8 of the fast slew rate 4'b001x: 1/4 of the fast slew rate 4'b0001: 1/2 of the fast slew rate

MFR_TRANS_FAST (FAh)

The MFR_TRANS_FAST command on Page 1 is used to set the Rail B reference fast slew rate when Rail B receives the SetVID_Fast_Up command. The REF down slew rate is set by the FDh register. Figure 22 shows the definition of the slew rate of VREF up and down (5mV/LSB). VID_STEP_NUM: FAh[7:6], VID_SR_CNT: FAh[5:0], ALERT_STEP_NUM: FDh[13:12], ALERT_SR_CNT: FDh[5:0].

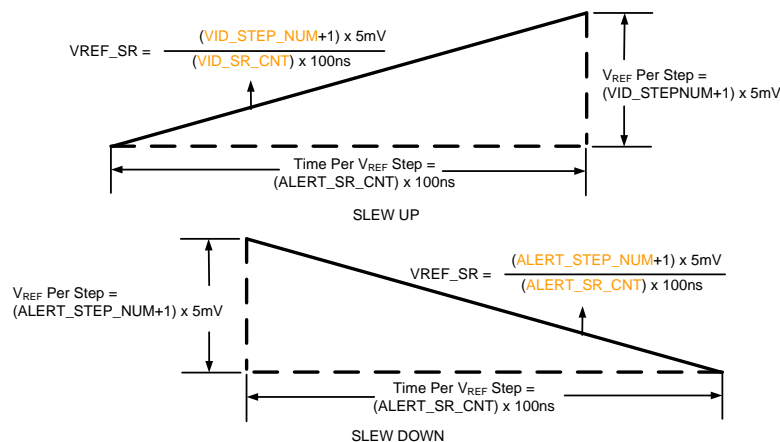


Figure 22: Slew Rate Definition

Normal slew rate = ([7:6]+1) * 5mV / ([5:0] * 100ns) * 10³ (mV/μs), in 5mV mode.

Normal slew rate = ([7:6]+1) * 10mV / ([5:0] * 100ns) * 10³ (mV/μs), in 10mV mode.

Command	MFR_TRANS_FAST															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VID_STEP_DECAY					MORE_RISING_STEP			VID_STEP_NUM		VID_SR_CNT					

Bits	Bit Name	Description
[15:14]	VID_STEP_DECAY	Sets the Rail B VID reference minus the step during decay. The step = 2 * bit[15:14] + 1.
[13]	SLP_S0_POS	Selection bit of the Rail B slew rate at the SLP_S0# positive edge at the ATOM platform. 1'b0: slow slew rate 1'b1: fast slew rate
[12]	SLP_S0_NEG	Selection bit of the Rail B slew rate at the SLP_S0# negative edge at the ATOM platform. 1'b0: slow slew rate 1'b1: fast slew rate
[11]	VID_SUBTRACT	Selection bit of the Rail B slew rate when the reference removes the additional rising step. 1'b0: 1/4 of the fast slew rate 1'b1: 1/8 of the fast slew rate
[10:8]	MORE_RISING_STEP	Sets the number of additional rising steps of Rail B after the VID reaches the target to increase the output voltage. Rising step = [10:8] * 2 + 1 in 5mV mode Rising step = [10:8] in 10mV mode
[7:6]	VID_STEP_NUM	Sets the Rail B reference step at one VID_SR_CNT period when slewing up. The step is equal to DEC([7:6]) + 1.
[5:0]	VID_SR_CNT	Sets the time length of Rail B that VREF changes once. 100ns/LSB.

MFR_EN_DLY (FBh)

The MFR_EN_DLY command on Page 1 is used to set the Rail B EN delay time.

Command	MFR_EN_DLY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	MFR_EN_DLY						

Bits	Bit Name	Description
[15:7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6:0]	MFR_EN_DLY	Sets the delay for Rail B to wait to output power after FBh[10:7] (on Page 0) passes, and there is no V _{IN} or temp fault. 20μs/LSB. This is the second delay for the start, and it is also the delay of hiccup, retry, and PMBus off and on.

MFR_IMON_SVID (FCh)

The MFR_IMON_SVID command on Page 1 is used to set the gain and offset of the Rail B I_{OUT} report from the VR to the SVID processor. R_{imon} can be calculated with Equation (15):

$$R_{imon} = \frac{1.6 * 8 * 32}{11 * K_{cs} * MFR_ICC_MAX} \quad (15)$$

Where K_{CS} is the Intelli-Phase current sense gain (in μA/A).

Command	MFR_IMON_SVID															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_IMON_SVID_OFFSET							MFR_IMON_SVID_GAIN							
Bits	Bit Name				Description											

[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:8]	MFR_IMON_SVID_OFF SET	Sets the Rail B I _{OUT} SVID report offset, which is added to the value directly to the SVID I _{OUT} report register (15h). The default value is 0. Bit[14] is the sign bit. If setting the offset to -1, set [14:8] = 7'h7F If setting the offset to -2, set [14:8] = 7'h7E
[7:0]	MFR_IMON_SVID_GAIN	Sets the gain of the Rail B I _{OUT} SVID report. The default value is 128.

MFR_ALT_SET (FDh)

The MFR_ALT_SET command on Page 1 is used to set the Rail B alert timing.

Slew rate of the alert reference: $([13:12] + 1) * 5\text{mV} / ([5:0] * 100\text{ns}) * 10^3 \text{ (mV/}\mu\text{s)}$, in 5mV mode.

Slew rate of the alert reference: $([13:12] + 1) * 10\text{mV} / ([5:0] * 100\text{ns}) * 10^3 \text{ (mV/}\mu\text{s)}$, in 10mV mode.

Command	MFR_ALT_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
[15:14]	ALERT_STEP_DECAY	Sets the VID decreasing step of Rail B during decay. The step is equal to $2 * \text{DEC} ([15:14]) + 1$.
[13:12]	ALER_STEP_NUM	Sets the VID decreasing step of Rail B at a non-decay DVID. The step is set to $\text{DEC} ([13:12]) + 1$.
[11]	SET_DACAY_FINISH	Selection bit for Rail B of when to pull the VR_settle signal high. 1'b0: wait for a set pulse after the decay is finished to pull the VR_settle signal high. 1'b1: does not wait for a set pulse after the decay is finished to pull the VR_settle signal high.
[10:6]	ALERT_DELAY_TIME	Sets the Rail B delay time to pull the VR_settle signal high after the alert reference reaches the target VID. 100ns/LSB.
[5:0]	ALERT_SR_CNT	Sets the Rail B time length of the alert reference changing one step. 100ns/LSB.

CLEAR_EEPROM_FAULTS (FEh)

The CLEAR_EEPROM_FAULTS command is used to clear the EEPROM fault bits. The VR starts ramping and outputs power if no other protection exists. This command is write only. There is no data byte for this command.

PAGE 2 REGISTER MAP

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor through only one physical address for the three rails and the test mode.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w
Function	X	X	X	X	X	X	PAGE	

Bits	Bit Name	Description
[7:2]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[1:0]	PAGE	2'b00: Page 0, all commands address Rail A 2'b01: Page 1, all commands address Rail B 2'b10: Page 2, all commands address Rail C Others: ineffective input

OPERATION (01h)

The OPERATION command on Page 2 is used to turn the device output on or off in conjunction with input from EN. OPERATION is also used to set the output voltage to the upper or lower margin voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of EN instructs the device to change to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OPERATION_MODE							

Bits	Bit Name	Description
[7:0]	OPERATION_MODE	Sets the operation mode for Rail C. 7'b00xxxxx: immediate off 7'b1000xxxx: normal on 7'b1001xxxx: margin low 7'b1010xxxx: margin high 7'b100101xx: margin low, ignore fault (ignore UV) 7'b101001xx: margin high, ignore fault (ignore OV2) The value of "x" does not matter.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set in Rail C. This command clears all bits in all status registers simultaneously. This command is write only. There is no data byte for this command.

CLEAR_LAST_FAULT (08h)

See the Page 0 LAST_FAULT_BLOCK (07h) section on page 33.

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus device to copy the Page 0 ~ Page 2 contents (not including read-only registers) of the operating memory to the matching locations in the MTP, regardless of the current PMBus register page. This command can be used while the device is outputting power. This command is write only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBus device to copy the Page 0 ~ Page 2 contents of the MTP to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the user store. Any items in the user store that do not have matching locations in the operating memory are ignored. It is *not* permitted to use this command while the device is outputting power unless MFR_EEPROM_COPY_EN (register 1Dh[1] in Page 0) is set to 1. This command is write only. There is no data byte for this command.

IDROOP_CTRL (1Bh)

The IDROOP_CTRL command on Page 2 is used to set the IDROOP DC gain for Rail C.

Command	IDROOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X		IDROOP_DC_SET			

Bits	Bit Name	Description																																				
[15:5]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.																																				
[4]	IDROOP_EN	Selection bit of the AC droop of Rail C. 1'b0: enable DC droop 1'b1: enable AC droop																																				
[3:0]	IDROOP_DC_SET	Sets the Rail C IDROOP DC gain to set the digital load line gain. The default value of 'Idroop_set' is 1 h.																																				
		<table><tr><th>Idroop_set[3:0]</th><th>Gain</th><th>Idroop_set[3:0]</th><th>Gain</th></tr><tr><td>0 h</td><td>0</td><td>8 h</td><td>11/8 * 1/8</td></tr><tr><td>1 h</td><td>4/8 * 1/8</td><td>9 h</td><td>12/8 * 1/8</td></tr><tr><td>2 h</td><td>5/8 * 1/8</td><td>A h</td><td>13/8 * 1/8</td></tr><tr><td>3 h</td><td>6/8 * 1/8</td><td>B h</td><td>14/8 * 1/8</td></tr><tr><td>4 h</td><td>7/8 * 1/8</td><td>C h</td><td>15/8 * 1/8</td></tr><tr><td>5 h</td><td>8/8 * 1/8</td><td>D h</td><td>16/8 * 1/8</td></tr><tr><td>6 h</td><td>9/8 * 1/8</td><td>E h</td><td>17/8 * 1/8</td></tr><tr><td>7 h</td><td>10/8 * 1/8</td><td>F h</td><td>18/8 * 1/8</td></tr></table>	Idroop_set[3:0]	Gain	Idroop_set[3:0]	Gain	0 h	0	8 h	11/8 * 1/8	1 h	4/8 * 1/8	9 h	12/8 * 1/8	2 h	5/8 * 1/8	A h	13/8 * 1/8	3 h	6/8 * 1/8	B h	14/8 * 1/8	4 h	7/8 * 1/8	C h	15/8 * 1/8	5 h	8/8 * 1/8	D h	16/8 * 1/8	6 h	9/8 * 1/8	E h	17/8 * 1/8	7 h	10/8 * 1/8	F h	18/8 * 1/8
		Idroop_set[3:0]	Gain	Idroop_set[3:0]	Gain																																	
		0 h	0	8 h	11/8 * 1/8																																	
		1 h	4/8 * 1/8	9 h	12/8 * 1/8																																	
		2 h	5/8 * 1/8	A h	13/8 * 1/8																																	
		3 h	6/8 * 1/8	B h	14/8 * 1/8																																	
		4 h	7/8 * 1/8	C h	15/8 * 1/8																																	
		5 h	8/8 * 1/8	D h	16/8 * 1/8																																	
		6 h	9/8 * 1/8	E h	17/8 * 1/8																																	
7 h	10/8 * 1/8	F h	18/8 * 1/8																																			

VOUT_COMMAND (21h)

The VOUT_COMMAND command on Page 2 sets the Rail C output voltage when the PMBus controls the output.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X		VOUT_COMMAND						

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VOUT_COMMAND	Sets the Rail C reference voltage (VID_DAC output voltage) in PMBus mode. In 5mV mode (E4h[5] = 1'b1): VREF = (VID + 49) / 2 * 5mV In 10mV mode (E4h[5] = 1'b0): VREF = (VID + 19) / 2 * 10mV

MFR_VOUT_TRIM (22h)

This MFR_VOUT_TRIM command on Page 2 is used to apply a fixed offset voltage to the Rail C output voltage command value for different power states. This command is most typically used by the end user to trim the output voltage at the time the PMBus device is assembled into the end user's system.

Command	MFR_VOUT_TRIM															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_TRIM_1_CCM				VOUT_TRIM_1_DCM			

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:4]	VOUT_TRIM_1_CCM	Applies a fixed offset voltage to the Rail C output voltage at 1-phase CCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.
[3:0]	VOUT_TRIM_1_DCM	Applies a fixed offset voltage to the Rail C output voltage at 1-phase DCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.

VOUT_CAL_OFFSET (23h)

The VOUT_CAL_OFFSET command on Page 2 offers an offset VID to the Rail C target determined by VOUT_COMMAND, VOUT_MARGIN_HIGH, and VOUT_MARGIN_LOW. This command is the initial value of the Rail C SVID offset.

Command	VOUT_CAL_OFFSET															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_CAL_OFFSET							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VOUT_CAL_OFFSET	Sets the VID offset in PMBus mode. It is also the initial value for the SVID offset register (33h). 5mV/LSB or 10mV/LSB according to E4h[5], -80h ~ +7Fh.

MFR_VOUT_MAX (24h)

The MFR_VOUT_MAX command on Page 2 is the Rail C initial value of SVID VOUT_MAX (SVID 30h), which sets an upper limit on the VID target (not including the offset) of SVID to provide a safeguard against an accidental setting of the output voltage to a possibly destructive level. If an attempt is made to program the VID target higher than VOUT_MAX, the command is rejected. The PMBus VID target is not constrained by MFR_VOUT_MAX.

Command	MFR_VOUT_MAX															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	MFR_VOUT_MAX							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	MFR_VOUT_MAX	Sets an upper limit on the Rail C VID target (not including the offset) of SVID.

VOUT_MARGIN_HIGH (25h)

The VOUT_ATOM_SLP_DEAST command on Page 2 is used to set the Rail C VID target when the SLP_S0# signal deasserts on the ATOM platform. The VOUT_MARGIN_HIGH command is used to set the Rail C reference voltage (VID_DAC output voltage) at the command MARGIN HIGH state.

Command	VOUT_MARGIN_HIGH															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VOUT_ATOM_SLP_DEAST								VOUT_MARGIN_HIGH							

Bits	Bit Name	Description
[15:8]	VOUT_ATOM_SLP_DEAST	Sets the Rail C reference voltage (VID_DAC output voltage) when SLP_S0# asserts in ATOM mode.
[7:0]	VOUT_MARGIN_HIGH	Sets the Rail C reference voltage (VID_DAC output voltage) at the command MARGIN HIGH state.

VOUT_MARGIN_LOW (26h)

The VOUT_ATOM_SLP_AST command on Page 2 is used to set the Rail C VID target when the SLP_S0# signal asserts on the ATOM platform. The VOUT_MARGIN_LOW command is used to set the Rail C reference voltage (VID_DAC output voltage) at the command MARGIN LOW state.

Command	VOUT_MARGIN_LOW															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VOUT_ATOM_SLP_AST								VOUT_MARGIN_LOW							

Bits	Bit Name	Description
[15:8]	VOUT_ATOM_SLP_AST	Sets the Rail C reference voltage (VID_DAC output voltage) when SLP_S0# deasserts in ATOM mode.
[7:0]	VOUT_MARGIN_LOW	Sets the Rail C reference voltage (VID_DAC output voltage) at the command MARGIN LOW state.

MFR_IMMEDIATE_SET (2Bh)

The MFR_IMMEDIATE_SET command on Page 2 sets the Rail C slew rate, alert time, and bit[0] of STATUS1 when SVID sends VID within $\pm 2\text{LSB}$ in 5mV mode.

Command	MFR_IMMEDIATE_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:8]	MFR_IMMED_REF_STEP	Sets the VID (output reference) step when SVID sends VID within $\pm 2\text{LSB}$ in 5mV mode of Rail C.
[7:5]	MFR_IMMED_ALT_TIME	Sets the time length of the ALTER slewing one step ($\text{FD}[13:12] + 1$) when SVID sends VID within $\pm 2\text{LSB}$ in 5mV mode of Rail C. 100ns/LSB.

[4:2]	MFR_IMMEDIATE_REF_TIME	Sets the time length of VID slewing one step ([9:8]) when the SVID sends VID within $\pm 2\text{LSB}$ in 5mV mode of Rail C. 100ns/LSB.
[1]	MFR_IMMEDIATE_SVID_EN	Enable bit of Rail C to force STATUS bit[0] to 1'b1. 1'b0: disable. STATUS bit[0] remains at 1'b0 until it settles normally. 1'b1: enable. Forces STATUS bit[0] to 1'b1 when the SetVID command is received within $\pm 2\text{LSB}$.
[0]	MFR_IMMEDIATE_REF_EN	Enable bit of Rail C for using bit[9:2]. 1'b0: disable 1'b1: enable

MFR_DEBUG (2Fh)

The MFR_DEBUG command on Page 2 is used to debug Rail C.

Command	MFR_DEBUG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r
Function	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X

Bits	Bit Name	Description
[15:2]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[1]	div2_en	Selects VDIFF to be above or below VREF 30mV or 15mV to trigger p30/n30. 1'b0: 30mV 1'b1: 15mV
[0]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.

IOUT_CAL_GAIN (38h)

The IOUT_CAL_GAIN command on Page 2 is used to set the Rail C PMBus I_{OUT} report gain and can be calculated with Equation (16):

$$\text{IOUT_CAL_GAIN} = \frac{K_{\text{CS}} * R_{\text{imon}} * 2^{15}}{32 * 1000 * k} \quad (16)$$

Where K_{CS} is the CS gain of the Intelli-Phase (in $\mu\text{A/A}$) (e.g.: MPS 86901C $K_{\text{CS}} = 10\mu\text{A/A}$), R_{imon} is the resistor connected to IMON (in $\text{k}\Omega$), and k is a coefficient according to ICCMAX.

Command	IOUT_CAL_GAIN															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	k					IOUT_CAL_GAIN										

Bits	Bit Name	Description
[15:11]	k	$k = 1$, IOUT_CAL_GAIN[15:11] = 5'b10001, when $20\text{A} \leq \text{ICCMAX}$ $k = 2$, IOUT_CAL_GAIN[15:11] = 5'b10010, when $10\text{A} \leq \text{ICCMAX} < 20\text{A}$ $k = 4$, IOUT_CAL_GAIN[15:11] = 5'b10011, when $5\text{A} \leq \text{ICCMAX} < 10\text{A}$
[10:0]	IOUT_CAL_GAIN	Sets the Rail C PMBus I _{OUT} report gain.

IOOUT_CAL_OFFSET (39h)

The IOOUT_CAL_OFFSET command on Page 2 is used to set the Rail C PMBus I_{OUT} report offset.

Command	IOOUT_CAL_OFFSET															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED						X	X	X	X	X	Mantissa				

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to -1 (dec) = 11111 (bin).
[10:6]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[5:0]	IOOUT_CAL_OFFSET	Signed value to set Rail C PMBus I _{OUT} report offset. 0.5A/LSB. Default value is 0. Bit[5] is the sign bit. For example, write 1111100000111110b = F83Eh to 39h to add -1A offset on the PMBus I _{OUT} report.

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 2 is a combined register of the output voltage fault flags for Rail C.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x	x			x	x	x
Default	0	x	x	0	0	x	x	x

Bits	Bit Name	Description
[7]		OVP flag. This bit is 1 if OVP is tripped.
[6]		Reserved.
[5]		Reserved.
[4]		UVP flag. This bit is 1 if UVP is tripped.
[3]		Vout_max_warning. The value written into PMBus 21h 25h/26h, which is larger than MFR_VOUT_MAX.
[2:0]		Reserved.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 2 is a combined register of the output current fault flags for Rail C.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x		x	x	x	x	x
Default	0	x	0	x	x	x	x	x

Bits	Bit Name	Description
[7]		OCF flag. This bit is 1 if OCF is tripped.
[6]		Reserved.
[5]		Phase current limit flag. This bit is 1 if the per-phase current limit is reached.
[4:0]		Reserved.

READ_VOUT (8Bh)

The READ_VOUT command on Page 2 is used to return the sensed VDIFF voltage of Rail C in VID format.

Command	READ_VOUT															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	X	READ_VOUT							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	READ_VOUT	Shows the sensed VDIFF voltage of Rail C in VID format.

READ_IOUT (8Ch)

The READ_IOUT command on Page 2 reflects the PMBus monitor Rail C total average output current.

Command	READ_IOUT(0.25A/LSB)															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	FIXED					READ_IOUT										

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to 11110 (bin) = -2 (dec).
[10:0]	READ_IOUT	Shows the total average output current of Rail C monitored by the PMBus. 0.25A/LSB.

READ_POUT (96h)

The READ_POUT command on Page 2 is used to monitor the Rail C output power.

Command	READ_POUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	READ_POUT								

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	READ_POUT	Shows the monitored output power of Rail C by the PMBus. 0.5W/LSB.

PS3_PS4_EXIT_DELAY (BEh)

The PS3_PS4_EXIT_DELAY command on Page 2 is used to set the time length of the VR to exit PS3/4. The format is the same as the SVID spec.

Command	PS3_PS4_EXIT_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PS3_EXIT_LATENCY_VR								PS4_EXIT_LATENCY_VR							

Bits	Bit Name	Description
[15:8]	PS3_EXIT_LATENCY_VR	Sets the time length (in μs) for Rail C to exit PS3. The time length is equal to $[11:8] / 16 * 2^{\wedge} [15:12]$.
[7:0]	PS4_EXIT_LATENCY_VR	Sets the time length (in μs) that VR takes to exit PS4. The time length is equal to $[3:0] / 16 * 2^{\wedge} [7:4]$.

DECAY_CFG_34H_06H (C2h)

The MUTI_VR_CONFIG command on Page 2 is the Rail C initial value of the SVID 34h register. The CAPABILITY_VR command on Page 2 is the bit mapped register, which identifies the SVID VR capabilities. The optional telemetry registers are supported.

Command	CFG_34H_06H															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MUTI_VR_CONFIG		CAPABILITY_VR							

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:8]	MUTI_VR_CONFIG	Initial value of the Rail C lower two bits of SVID MUTI_VR_CONFIG (34h).
[7:0]	CAPABILITY_VR	Shows which of the telemetry registers Rail C supports. A 1 in any bit indicates that an optional function is supported by the slave. Bit[7]: I _{OUT} /J _{OUT} format (15h) Bit[6]: temperature (17h) Bit[5]: input P (1Bh) Bit[4]: input V (1Ah) Bit[3]: input I (19h) Bit[2]: P _{OUT} (18h) Bit[1]: V _{OUT} (16h) Bit[0]: I _{OUT} (15h)

TOLERANCE_SR_FAST (C3h)

The MFR_VR_TOLERANCE command on Page 2 is used to set the Rail C output tolerance (binary format in mV). The SR_FAST_VR command on Page 2 is used to set the data register containing the Rail C fast slew rate capability of the slew rate the platform VR can sustain (binary format in mV/ μs).

Command	TOLERANCE_SR_FAST															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_VR_TOLERANCE								SR_FAST_VR							

Bits	Bit Name	Description
[15:8]	MFR_VR_TOLERANCE	Shows the Rail C output tolerance. 1mV/LSB.
[7:0]	SR_FAST_VR	Shows the fast slew rate that Rail C supports. 1mV/ μs per LSB.

MFR_VOUT_MAX_9BIT (C4h)

The MFR_VOUT_MAX_9BIT command on Page 2 is used to set the Rail C upper limit of VID + OFFSET. In PMBus mode, if VID + OFFSET is higher than this limit, the command is acknowledged, and the output is latched at this limit. In SVID mode, if VID + OFFSET is higher than this limit, this command is rejected, and the output holds the voltage before the command.

Command	MFR_VOUT_MAX_9BIT															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	MFR_VOUT_MAX_9BIT								

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	MFR_VOUT_MAX_9BIT	Sets the Rail C upper limit of VID + OFFSET.

IVID2_1_I_DEF (C5h)

The ivid2_i_def command on Page 2 is the default value of the Rail C maximum current (1A/bit) expected when VID is set as IVID2 - VID \geq VID > IVID3 - VID. The ivid1_i_def command on Page 2 is the Rail C default value of the maximum current (1A/bit) expected when the VID is set as IVID1 - VID \geq VID > IVID2 - VID.

Command	IVID2_1_I_DEF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Ivid2_i_def								Ivid1_i_def							

Bits	Bit Name	Description
[15:8]	Ivid2_i_def	Sets the Rail C default value of the maximum current expected when VID is set as IVID2 - VID \geq VID > IVID3 - VID. 1A/LSB.
[7:0]	Ivid1_i_def	Sets the Rail C default value of the maximum current expected when VID is set as IVID1 - VID \geq VID > IVID2 - VID. 1A/LSB.

PIN_MAX_IVID3_I_DEF (C6h)

The ivid3_i_def is the Rail C default value of the maximum current (1A/bit) expected when VID is set as IVID3 - VID \geq VID.

Command	PIN_MAX_IVID3_I_DEF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	Ivid3_i_def (1A/LSB)							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	Ivid3_i_def	Sets the Rail C default value of the maximum current expected when VID is set as IVID3 - VID \geq VID. 1A/LSB.

DC_CTRL_ADP_CTRL (CCh)

The MFR_DC_CTRL command on Page 2 is used to hold the DC loop and bypass the SET_PS command for Rail C.

Command	DC_CTRL_ADP_CTRL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	MFR_DC_CTRL				
Bits	Bit Name				Description											
[15:5]	RESERVED				Unused. X indicates that writes are ignored and always read as 0.											
[4]	MFR_DC_CTRL[3]				Holds the Rail C DC loop for a given time, CBh[14:11], when the frequency is lower than that set by CFh[8:0], and VID is lower than that set by CBh[7:0] under PS0/PS1 (related register in Page 0). 1b'1: hold DC loop if CCh[10] = 1, enable DC loop if CCh[10] = 0 1b'0: enable DC loop if CCh[10] = 1, enable DC loop if CCh[10] = 0											
[3]	MFR_DC_CTRL[2]				Enable bit for Rail C to hold the DC calibration during the load transient. 1'b0: disable 1'b1: enable											
[2]	MFR_DC_CTRL[1]				Enable bit for Rail C to hold the DC calibration during Set_PS, decay, and SetVID_Fast/Slow. 1'b0: disable 1'b1: enable											
[1]	MFR_DC_CTRL[0]				Enable bit for Rail C to hold the DC calibration when the PWM frequency is lower than that set by CFh[8:0] or the PWM frequency is higher than that set by CDh[13:6] during CCM. 1'b0: disable 1'b1: enable											
[0]	MFR_ADP_PSI_BYPASS				Disables the Rail C Set_PS command when auto-phase shedding is enabled (not including IVID). 1'b0: enable 1'b1: disable											

HF_PFM_SLP_DISCHG (CDh)

The DISCHG_NUM command on Page 2 is used to set the slope ramp discharge MOSFET number of Rail C.

Command	HF_PFM_SLP_DISCHG															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	X	X	DISCHG_NUM		

Bits	Bit Name	Description
[15:3]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[2:0]	DISCHG_NUM	Sets the Rail C internal slope ramp discharge MOSFET number.

MFR_TRIM_2_1_DCM (DEh)

The MFR_TRIM_2_1_DCM command on Page 2 is used to trim the Rail C output voltage during 1-phase ~ 2-phase CCM and 1-phase DCM.

Command	MFR_TRIM_2_1_DCM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_TRIM_2					MFR_TRIM_1					MFR_TRIM_DCM				

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:10]	MFR_TRIM_2	Sets the Rail C V_{OUT} trim for 2-phase CCM operation. 2.73mV/LSB.
[9:5]	MFR_TRIM_1	Sets the Rail C V_{OUT} trim for 1-phase CCM operation. 2.73mV/LSB.
[4:0]	MFR_TRIM_DCM	Sets the Rail C V_{OUT} trim for 1-phase DCM operation. 2.73mV/LSB.

VTRIM_STEP_VCAL_PI (E3h)

The MFR_VCAL_PI command on Page 2 is used to set the Rail C PI value for DC calibration.

Command	VTRIM_STEP_VCAL_PI															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	MFR_VCAL_PI						

Bits	Bit Name	Description
[15:7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6:0]	MFR_VCAL_PI	Sets the PI parameter for DC loop calibration for Rail C.

MFR_VR_CONFIG (E4h)

The MFR_VR_CONFIG command on Page 2 is used to enable the function of Rail C, such as DC loop calibration, etc.

Command	MFR_VR_CONFIG															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X											
Bits	Bit Name		Description													
[15:11]	RESERVED		Unused. X indicates that writes are ignored and always read as 0.													
[10]	MFR_PMBUS_SR_SEL		Selection bit of Rail C for the VID slew rate when the PMBus controls V_{OUT} . 1b'0': V_{OUT} changes with a fast slew rate when the PMBus controls V_{OUT} . 1b'1': V_{OUT} changes with a slow slew rate when the PMBus controls V_{OUT} .													
[9]	DC_LOOP_DCM_EN		Enable bit for Rail C DC calibration during PS2. Only active when DC_LOOP_EN is enabled. 1b'0': disable 1b'1': enable when bit[10] = 1													
[8]	DC_LOOP_EN		Enable bit for the Rail C DC calibration. 1b'0': disable 1b'1': enable DC calibration in CCM. Must enable bit[11] for PS2 DC calibration.													

[7]	PMBUS_PS_EN	Enable bit for the PMBus to control the power state of Rail C in PMBus mode. 1'b0: disable 1'b1: enable
[6:5]	PMBUS_PS	Sets the Rail C power state when the PMBus forces the power state. 2'b00: PS0 2'b01: PS1 2'b10: PS2 2'b11: PS3
[4]	TON_REDUCTION_DCM_EN	Enable bit of Rail C to reduce the PS2 on time to 75% of that in PS0. 1'b0: disable 1'b1: enable
[3]	VID_STEP	Selection bit of the VID step for Rail C. 1'b1: 5mV/LSB 1'b0: 10mV/LSB
[2]	APS_EN	Enable bit of Rail C auto-phase shedding function. 1'b0: disable 1'b1: enable
[1]	IVID_EN	Enable bit of Rail C IVID function. 1'b0: disable 1'b1: enable
[0]	PMBUS_MODE_SEL	Selection bit of Rail C controlled by the PMBus or SVID. 1'b0: SVID 1'b1: PMBus

MFR_FS_VBOOT (E5h)

The MFR_FS_VBOOT command on Page 2 is used to set the boot-up voltage for Rail C.

Command	MFR_FS_VBOOT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	MFR_VBOOT							
Bits	Bit Name				Description											
[15:8]	RESERVED				Unused. X indicates that writes are ignored and always read as 0.											
[7:0]	MFR_VBOOT				Sets the boot-up voltage for Rail C (VID format). For example, to set the output voltage at 0.9V, set E5h [7:0] = 8'h83 (5mV VID mode) or 8'h47 (10mV VID mode).											

VFB_TRIM_DCLL (E7h)

The VFB_TRIM_DCLL command on Page 2 is used to record the VFB buffer trim without the IDROOP and DC load line of Rail C.

Command	VFB_TRIM_DCLL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	VFB buffer trim without IDROOP						DC load line, 0.1mohm/LSB							

Bits	Bit Name	Description
[15:14]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[13:8]	VFB buffer trim without IDROOP	Records the Rail C VFB buffer trim without IDROOP.
[7:0]	DC load line	Records the Rail C DC load line. 0.1mΩ/LSB.

MFR_CUR_GAIN (E9h)

The MFR_CUR_GAIN command on Page 2 is used to set the per-phase current sense gain of Rail C. Calculate I_{READ} with Equation (17):

$$I_{READ} = \frac{I_{CS} * K_{CS} * R_{CS} + 1.23}{32 * MFR_CUR_GAIN} * 1023 - MFR_CUR_OFFSET \quad (17)$$

Where K_{CS} is in $\mu A/A$, and R_{CS} is in Ω .

Command	MFR_CUR_GAIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_CUR_GAIN									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_CUR_GAIN	Sets the gain of the per-phase current sense of Rail C. MFR_CUR_GAIN is used to calculate the current from the per-phase current sample results.

MFR_CUR_OFFSET (EAh)

The MFR_CUR_OFFSET command on Page 2 is used to set the offset for the Rail C 1.23V bias voltage of the per-phase current sense.

Command	MFR_CUR_OFFSET							
Format	signed binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_CUR_OFFSET							

Bits	Bit Name	Description
[7:0]	MFR_CUR_OFFSET	Sets the offset for the 1.23V bias voltage of the per-phase current sense.

MFR_OCP_SET_LEVEL (EEh)

The MFR_OCP_SET_LEVEL command on Page 2 is used to set the Rail C OC limit level.

Command	MFR_OCP_SET_DELAYTIME, MFR_OCP_SET_LEVEL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	MFR_OCP_SET_LEVEL						

Bits	Bit Name	Description
[15:7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6:0]	MFR_OCP_SET_LEVEL	Sets the Rail C over-current limit value (1A/LSB). The total OCP limit is set at [6:0]*phase num, which is compared with READ_IOUT(8Ch)/4.

OCP_LIMIT_ICC_MAX (EFh)

The OCP_DA_LIMIT on Page 2 is used to set the single-phase valley current limit of Rail C. The MFR_ICC_MAX command on Page 2 is used to set the ICCMAX of Rail C.

Command	OCP_LIMIT_ICC_MAX															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OCP_DA_LIMIT								MFR_ICC_MAX							

Bits	Bit Name	Description
[15:8]	OCP_DA_LIMIT	Sets the valley limitation level of the current sense (CS) of single-phase for Rail C. 10mV/LSB. The MP2949A will not latch when it reaches the limit and usually ends in UVP.
[7:0]	MFR_ICC_MAX	Sets the ICCMAX for Rail C. 1A/LSB. 00h indicates that this value is not programmed and the platform will not boot.

UVP_OVP_OCP_MODE (F1h)

The UVP_OVP_OCP_MODE command on Page 2 is used to set the platform time and the UV/OV/OC protection mode of Rail C.

Command	UVP_OVP_OCP_MODE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_PLATFORM TIME											
Bits	Bit Name				Description											
[15:12]	RESERVED				Unused. X indicates that writes are ignored and always read as 0.											
[11:6]	MFR_PLATFORM_TIME				Sets the period after VID has added the rising step and before VID starts to subtract the rising step of Rail C. 0.5µs/LSB.											
[5:4]	MFR_UVP_SET_MODE				Sets the Rail C UVP mode. 2'b00: no action 2'b01: latch 2'b01: hiccup 2'b11: retry six times and then latch off											
[3:2]	MFR_OVP_SET_MODE				Sets the Rail C OVP2 mode. 2'b00: no action 2'b01: latch 2'b01: hiccup 2'b11: retry six times and then latch off											

[1:0]	MFR_OCP_SET_MODE	Sets the Rail C OCP mode. 2'b00: no action 2'b01: latch 2'b01: hiccup 2'b11: retry six times and then latch off
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MFR_FIXED_OVP_SET (F6h)

The MFR_FIXED_OVP_SET command on Page 2 is used to set the Rail C OVP1 level.

Command	MFR_FIXED_OVP_SET							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_FIXED_OVP_SET							

Bits	Bit Name	Description
[7]	Bit[7]	Sets the Rail C OVP1 level. 1'b0: OVP1 limitation is set at 0V 1'b1: OVP1 limitation depends on bit[6:0].
[6:0]	MFR_FIXED_OVP_SET	Sets the Rail C OVP1 level. Once the sensed V_{OUT} (VDIFF) is over this level, the VR is protected. 20mV/LSB. For example, to set the OVP1 level at 1.92V, set F6h = 8'hB0 for the 1/2 buffer on the remote sense.

MFR_FILTER_SET (F9h)

The MFR_FILTER_SET on Page 2 is used to set the parameters of the VID filter and slow the slew rate for Rail C.

Command	MFR_FILTER_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X					SLOW_SR_SEL			
Bits	Bit Name				Description											
[15:8]	RESERVED				Unused. X indicates that writes are ignored and always read as 0.											
[7]	MFR_DAC_CMP_EN				Enable bit of DAC_CMP_FILTER from the analog of Rail C, which is used to filter the VID_DAC output until the filtered VID_DAC output level equals the VID_DAC output when SetVID_down is interrupted by SetVID_up. 1'b0: disable 1'b1: enable											
[6]	MFR_VID_FILTER_EN				Enable bit of the VID filter for Rail C, which is the VID DAC output filter when SetVID_fast/slow_down transitions. There is no VID filter when VID is up or VID is down by decay. Set PS4 CMD. 1'b0: disable 1'b1: enable											
[5:4]	MFR_VID_FILTER				Sets the Rail C VID_DAC output filter. 2'b00: 1μs added filter at VID ramping down or steady V _{OUT} 2'b01: 3μs added filter at VID ramping down or steady V _{OUT} 2'b10: 5μs added filter at VID ramping down or steady V _{OUT} 2'b11: 7μs added filter at VID ramping down or steady V _{OUT}											
[3:0]	SLOW_SR_SEL				Selection bit of the slew rate when Rail C receives the SetVID_Slow command. 4'b1xxx: 1/16 of the fast slew rate 4'b01xx: 1/8 of the fast slew rate 4'b001x: 1/4 of the fast slew rate 4'b0001: 1/2 of the fast slew rate											

MFR_TRANS_FAST (FAh)

The MFR_TRANS_FAST command on Page 2 is used to set the Rail C reference fast slew rate when Rail C receives the SetVID_Fast_Up command. The REF down slew rate is set by the FDh register. Figure 23 shows the definition of the slew rate of VREF up and down (5mV/LSB). VID_STEP: FAh[7:6], VID_SR_CNT: FAh[5:0], ALERT_STEP_NUM: FDh[13:12], ALERT_SR_CNT: FDh[5:0].

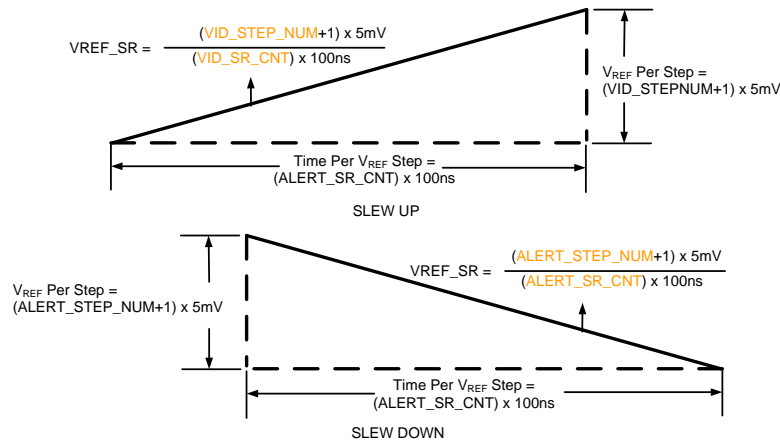


Figure 23: Slew Rate Definition

Normal slew rate = ([7:6]+1) * 5mV / ([5:0]*100ns) * 10³ (mV/μs), in 5mV mode.

Normal slew rate = ([7:6]+1) * 10mV / ([5:0]*100ns) * 10³ (mV/μs), in 10mV mode.

Command	MFR_TRANS_FAST															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VID_STEP_DECAY					MORE_RISING_STEP			VID_STEP_NUM		VID_SR_CNT					
Bits	Bit Name				Description											
[15:14]	VID_STEP_DECAY				Sets the Rail C VID reference minus the step during decay. The step = 2*bit[15:14]+1.											
[13]	SLP_S0_POS				Selection bit of the Rail C slew rate at the SLP_S0# positive edge at the ATOM platform. 1'b0: slow slew rate 1'b0: fast slew rate											
[12]	SLP_S0_NEG				Selection bit of the Rail C slew rate at the SLP_S0# negative edge at the ATOM platform. 1'b0: slow slew rate 1'b0: fast slew rate											
[11]	VID_SUBTRACT				Selection bit of the Rail C slew rate when the reference removes the additional rising step. 1'b0: 1/4 of the fast slew rate 1'b1: 1/8 of the fast slew rate											
[10:8]	MORE_RISING_STEP				Sets the number of additional rising steps of Rail 3 after the VID reaches the target to increase the output voltage. Rising step = [10:8] * 2 + 1 in 5mV mode Rising step = [10:8] in 10mV mode											
[7:6]	VID_STEP_NUM				Sets the Rail C reference step at one VID_SR_CNT period when slewing up. The step is equal to DEC([7:6]) + 1.											
[5:0]	VID_SR_CNT				Sets the time length of Rail C that VREF changes once. 100ns/LSB.											

MFR_EN_DLY (FBh)

The MFR_EN_DLY command on Page 2 is used to set the Rail C EN delay time.

Command	MFR_EN_DLY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	MFR_EN_DLY						

Bits	Bit Name	Description
[15:7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6:0]	MFR_EN_DLY	Sets the delay for Rail C to wait to output power after FBh[10:7] (on Page 0) passes, and there is no V _{IN} or temp fault. 20μs/LSB. This is the second delay for the start, and it is also the delay of hiccup, retry, and PMBus off and on.

MFR_IMON_SVID (FCh)

The MFR_IMON_SVID command on Page 2 is used to set the gain and offset of the Rail C I_{OUT} report from the VR to the SVID processor. R_{imon} can be calculated with Equation (18):

$$R_{imon} = \frac{1.6 \times 8 \times 32}{11 \times K_{cs} \times \text{MFR_ICC_MAX}} \quad (18)$$

Where K_{CS} is the Intelli-Phase current sense gain (in μA/A).

Command	MFR_IMON_SVID															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_IMON_SVID_OFFSET								MFR_IMON_SVID_GAIN						

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:8]	MFR_IMON_SVID_OFFSET	Sets the Rail C I _{OUT} SVID report offset, which is added to the value directly to the SVID I _{OUT} report register (15h). The default value is 0. Bit[14] is the sign bit. If setting the offset to -1, set [14:8] = 7'h7F If setting the offset to -2, set [14:8] = 7'h7E
[7:0]	MFR_IMON_SVID_GAIN	Set the gain of the Rail C I _{OUT} SVID report. Default value is 128.

MFR_ALT_SET (FDh)

The MFR_ALT_SET command on Page 2 is used to set the Rail C alert timing.

Slew rate of the alert reference: ([13:12] + 1) * 5mV / ([5:0]*100ns) * 10³ (mV/μs), in 5mV mode.

Slew rate of the alert reference: ([13:12] + 1) * 10mV / ([5:0]*100ns) * 10³ (mV/μs), in 10mV mode.

Command	MFR_ALT_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
[15:14]	ALERT_STEP_DECAY	Sets the VID decreasing step of Rail C during decay. The step is equal to 2 * DEC ([15:14]) + 1.

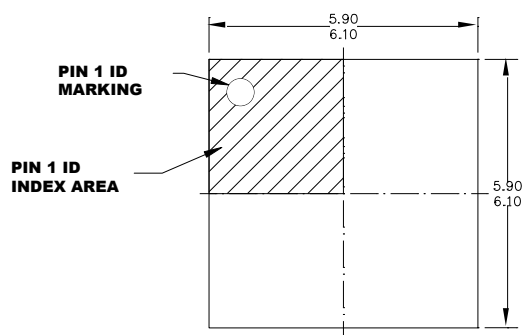
[13:12]	ALER_STEP_NUM	Sets the VID decreasing step of Rail C at a non-decay DVID. The step is set to DEC ([13:12]) + 1.
[11]	SET_DACAY_FINISH	Selection bit of Rail C of when to pull the VR_settle signal high. 1'b0: waits for a set pulse after decay finishes to pull the VR_settle settle signal high. 1'b1: does not wait for a set pulse after decay finishes to pull the VR_settle signal high..
[10:6]	ALERT_DELAY_TIME	Sets the Rail C delay time to pull the VR_settle signal high after the alert reference reaches the target VID. 100ns/LSB.
[5:0]	ALERT_SR_CNT	Sets the Rail C time length of the alert reference changing one step. 100ns/LSB.

CLEAR_EEPROM_FAULTS (FEh)

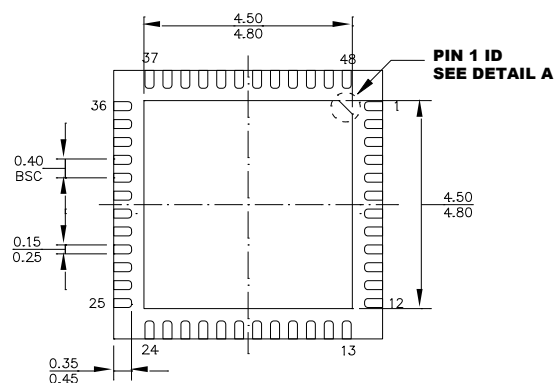
The CLEAR_EEPROM_FAULTS command is used to clear the EEPROM fault bits. The VR starts ramping and outputs power if no other protection exists. This command is write only. There is no data byte for this command.

PACKAGE INFORMATION

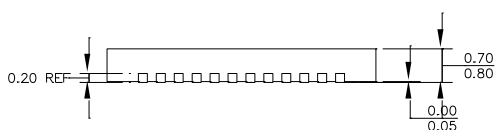
TQFN-48 (6mmx6mm)



TOP VIEW

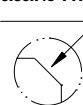


BOTTOM VIEW



SIDE VIEW

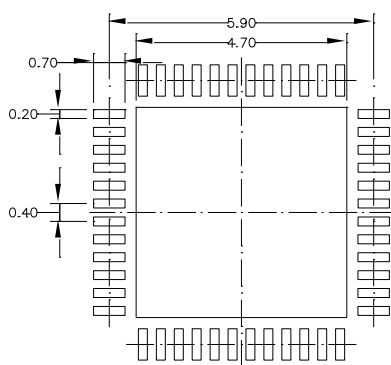
PIN 1 ID OPTION A
0.30x45° TYP.



PIN 1 ID OPTION B
R0.25 TYP.



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220, VARIATION VJJE-1.
- 5) DRAWING IS NOT TO SCALE.

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